

Five Important ESD Protection Considerations for Augmented Reality Wearables

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How to design for safety, reliability, and connectivity using the latest circuit protection technologies and board layout strategies.

Those of us who wear vision correction glasses are used to seeing the world through lenses. New technologies will allow a virtual world to be layered on top of the real world that we normally see. The lenses will become displays that allow us to see the “real” world that is augmented with overlaid information and images, creating an Augmented Reality (AR). An example would be the integration of navigation into the AR glasses to allow a user to walk through town with turn-by-turn instructions (visual or verbal) to help them easily get to their destination. Other examples include facial recognition, fitness tracking, first-person photos and videos, as well as health-sensing and travel applications (Figure 1).



Figure 1: Augmented Reality (AR) glasses displaying airline flight information.

This article will discuss advanced circuit protection technologies and board layout strategies that safeguard wearable devices and their users. Applying these recommendations early in the design process will help today’s circuit designers improve the performance, safety, and reliability of their wearable technology designs and help build a more reliable IoT ecosystem.

Wearables ESD considerations: selection and configuration factors for TVS Diodes

1. Small form factor

Today’s ESD diodes offer a variety of performance benefits for Augmented Reality applications led by a small form factor (Figures 2 and 3). The following recommendations for the selection and configuration of ESD Diode technologies will help design engineers optimize their future circuit designs.

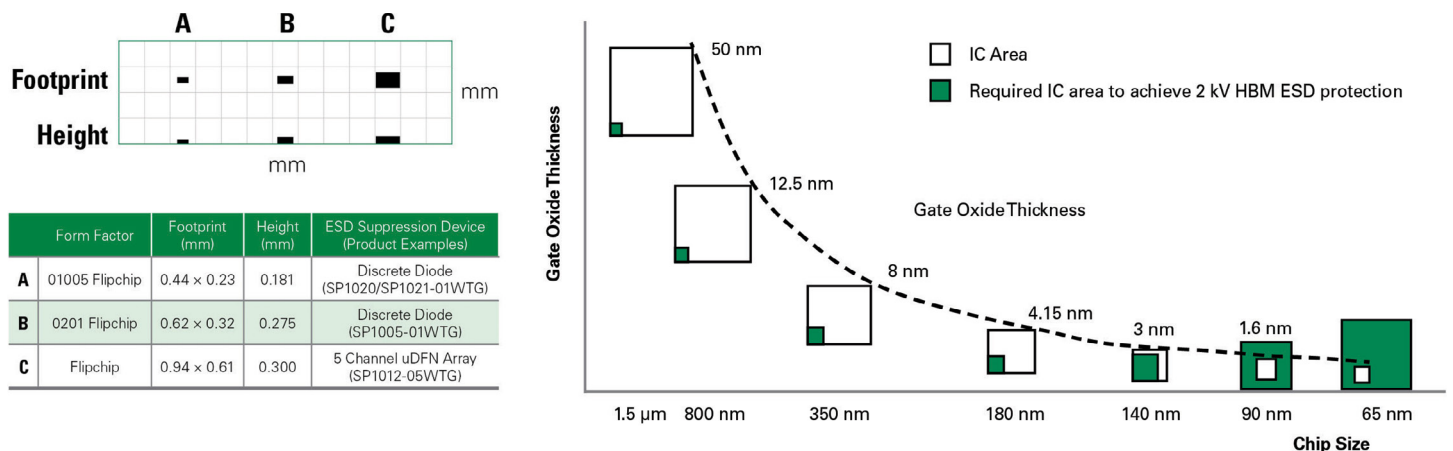


Figure 2: As the sophisticated chipsets used in wearable devices get smaller, the form factor, required IC area, and circuit protection devices must do the same.

2. Choosing unidirectional or bidirectional diodes

ESD diodes are available in unidirectional or bidirectional configurations. Unidirectional diodes are typically used for DC circuits, including pushbuttons and keypads, as well as digital circuits. Bidirectional diodes are used in AC circuits, which may include any signal with a negative component greater than $-0.7V$. These circuits include audio, analog video, legacy data ports and RF interfaces.

Whenever possible, design engineers should choose unidirectional diode configurations to improve performance during negative-voltage ESD strikes. During these strikes, the clamping voltage will be based on the forward bias of the diode, which is typically less than $1.0V$. A bidirectional diode configuration provides a clamping voltage during a negative strike that is based on the reverse breakdown voltage, which is higher than the forward bias of the unidirectional diode. Thus, the unidirectional configuration can dramatically reduce the stress on the system during negative transients.

3. Determine diode location

Most circuits do not need board-level ESD Diodes at each of the IC's pins. Rather, the designer should determine which pins have exposure to the outside of the application where user-generated ESD events are likely to occur. If the communication/control line can be touched by the user, it could become a pathway for ESD to enter the integrated circuit. Typical circuits include USB, audio, buttons, switches, RF antennas, and other data buses. Incrementally adding these discrete devices will take up board space, so it is important to reduce their size to fit 0201 or 01005 outlines. For some wearable applications, there are also space-saving multi-channel arrays available. It is generally recommended to put the ESD device as close to the ESD ingress point as possible, which is typically defined as the connector or the I/O.

4. Consider routing of "ESD" trace

To protect the IC's pins with an ESD Diode, there are several key considerations for trace routing—from I/O to ground. Unlike lightning transients, ESD does not unleash a large amount of current for a long duration of time. To effectively handle ESD, it is important to move the charge from the protected circuit to the ESD reference as quickly as possible. The length of the trace—from the I/O line to the ESD component and from the ESD component to ground—are the overriding factors, not the width of the trace to ground. The length of the trace should be kept as short as possible to limit parasitic inductance. This inductance would result in inductive overshoot, which is a brief voltage spike that can reach hundreds of volts if the stub trace is long enough. Recent package developments include μ DFN and Wafer Level Chip Scale Packages (WLCSP) outlines that fit directly over the data lanes to eliminate the need for stub traces entirely.

5. Understand HBM, Machine Model (MM) and Charged Device Model (CDM) definitions

HBM, MM, and CDM are test models for characterizing the ESD robustness of the integrated circuits that run the portable device or wearable, including the processor, memory, and ASIC. They are used by the semiconductor supplier to ensure the robustness of the circuits during manufacturing. The current trend is for suppliers to reduce the voltage test levels since it saves die space. Additionally, most electronics manufacturers have provisioned for ESD and have countermeasures in place during the assembly process.



Figure 3: Products like the SP1020 from Littelfuse pack robust ESD protection in a very space efficient 01005 package; ideal for applications like AR Glasses where there is very little board space available.



Figure 4: Low-capacitance bidirectional discrete TVS diode arrays, including the SP3522 Series, provide symmetrical ESD protection for high-speed data lines when AC signals are present. They are also designed for consumer electronics such as fitness bands, smartwatches, smartphones, tablets and eReaders.

If ESD protection is only provisioned for during assembly, then once the device reaches the consumer, the device is susceptible to ESD damage in the consumer's environment. Electronics devices without adequate ESD countermeasures built into the unit will fail incrementally or catastrophically in the user's environment. To guarantee happy customers and fewer ESD related field failures, the designer must select a board-level device that is robust enough to protect against intense electrical stresses yet offers the bandwidth and the electrical performance demanded by the end-user product. When evaluating an ESD protection device, consider the following parameters:

- Dynamic resistance: Defines the diode's resistance to the change in state from blocker to conduit of electronic energy. This value is a demonstration of how fast the diode will clamp and divert the ESD transient pulse to ground. It helps show how efficiently the avalanche diode conducts the excess voltage and current to ground. The more vertical the I-V or TLP curve is, the more efficient the avalanche diode is, and the lower the expressed dynamic resistance.
- IEC 61000-4-2 rating: Tested and confirmed during design and characterization, this rating reflects what the ESD diode is capable of withstanding repeatedly without degradation of the DC performance. For this parameter, typically, the higher the value, the better. A growing number of Littelfuse ESD Diodes approach 20kV and 30kV under contact discharge conditions, which regularly exceeds industry standards for fielded electronics, nominally 8kV air discharge.
- DC (Direct Current) Performance: There are several important considerations when designing circuits that need protection:
 - Surge tolerance (8/20us),
 - Parasitic capacitance,
 - Parasitic inductance, and
 - Nominal and maximum leakage currents.

Approaches vary depending upon the performance characteristics of the interfaces which are being protected.

For additional information on ESD protection for wearable devices, you can download our [ESD Suppression Design Guide and Wearables Protection Application Note](#), courtesy of Littelfuse, Inc.

About the author



Todd Phillips is the Global Strategic Marketing Manager for the Electronics Business Unit. He joined Littelfuse as a sales engineer in 2006 for the industrial business unit. Todd joined the electronics business unit in 2011 as a regional sales manager. His current responsibilities include the development of marketing collateral material, management of marketing activities for new product launches, and performing market studies and feasibility analyses for new product ideas. He received his BSEE from Milwaukee School of Engineering. Todd can be reached at tphillips@littelfuse.com.

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