



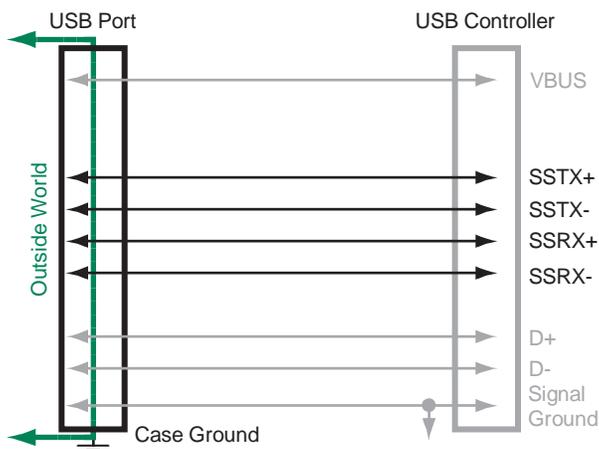
The Universal Serial Bus (USB) was released in 1996 to standardize connections between computer peripherals; more than 3.5 billion USB devices are expected to ship in 2012.

In 2010, the first devices with USB 3.0 interfaces were introduced, reaching about 100 million units. This number increased rapidly in 2012 (and is now forecasted to approach 500 million devices) as the SuperSpeed protocol became a native connection in the newest chipsets.

USB 3.0 devices incorporate four additional data channels providing 5Gbps communication speeds and the power bus has been up-rated to 900mA maximum current. These new USB 3.0 specifications, combined with continuous shrinkage of integrated chip geometries, make protection against electrical transients and overcurrent faults more critical and more complicated. The threats of damage are higher, even from smaller electrostatic discharges (ESDs), as well as from short circuit events.

With faster throughput and greater chip sensitivity, signal integrity and system reliability should be of greater concern for systems designers. Parasitic capacitance, low clamping voltage and low resistance become key criteria in circuit protection component selection. Due to the higher currents available on Vbus, a lower resistance of the overcurrent protector also becomes critical to ensure low voltage drop.

Understanding key selection criteria and tradeoffs between protection technologies (PTCs, varistors, and polymer and silicon-based devices) is key to achieving a successful design. This application note explains factors and issues that require consideration in detail.



**Fig. 1: USB 3.0 adds dual differential data pairs.**

## USB 3.0 Operating Characteristics

The Universal Serial Bus (USB) standard is a set of interface specifications for high speed wired communication between electronic systems. The USB 3.0 standard specifies increased data transfer rates, increased power output, and maintains backward compatibility with USB 2.0.

The most significant physical change from USB 2.0 to USB 3.0 has been the introduction of two differential data pairs called SSRx+/SSRx- and SSTx+/SSTx- to run in parallel with the existing D-/D+ data bus. This allows full duplex simultaneous transfer of data as opposed to the single duplex unidirectional USB 2.0 bus.

USB 3.0 also included an increase in available current on Vbus from 500mA to 900mA, which expands the options for powering external devices, eliminating the need for extra power supplies.

## USB 3.0 Circuit Protection Challenges

With the increase in data transfer rate to 5Gbps and required decrease in channel capacitance in order support the new data rate, the ESD protection used in previous generations of USB may be inadequate for use with USB 3.0. Designers are more challenged to find voltage transient protection solutions that can protect sensitive data lines without adding signal distorting capacitance.

The introduction of additional differential data pairs requires more data lines to be protected against ESD and discrete ESD protection solutions used in the past to protect each individual data line may not be the ideal solution. New silicon array ESD protection devices, which are placed directly on the data pairs, not only protect legacy USB 2.0 data lines but also these additional data signal pairs.

For over-current protection, USB 3.0 Specification Section 11.4.1.1.1 states:

*The host and all self-powered hubs must implement over-current protection for safety reasons, and the hub must have a way to detect the over-current condition and report it to the USB software.*

*The over-current limiting mechanism must be resettable without user mechanical intervention. Polymeric PTCs and solid-state switches are examples of methods that can be used for over-current limiting.*

Overcurrent protection may also be required in some equipment per UL60950-1.

## Overcurrent Protection

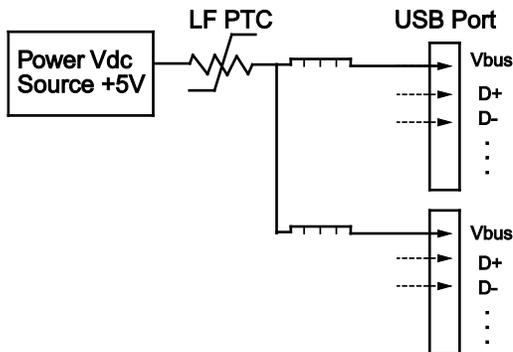
USB Bus Transceiver ICs (integrated circuits) or Power Management ICs may include some current limiting functions; however, when the ICs do not include current limiting features or when supplemental protection is required, the circuit designer must use current limiting PTCs for the Vbus.

Installing a Polymeric PTC device on Vbus (see Figure 7) limits current in the event of a short circuit, and prevents overcurrent damage caused by the sudden short circuit. It may also help achieve UL60950-1 compliance to Sec 2.5 (Limited Power Source, Table 2B), which states that short circuit current must be limited to less than 8A in 5 sec.

Related to USB hub applications, the USB 3.0 over-current protection specification 11.4.1.1.1 states:

*Should the aggregate current drawn by a gang of downstream facing ports exceed a preset value, the over-current protection circuit removes or reduces power from all affected downstream facing ports. The preset value cannot exceed 5.0A and must be sufficiently higher than the maximum allowable port current or time delayed such that transient currents (e.g., during power up or dynamic attach or reconfiguration) do not trip the over-current protector.*

Figure 2 shows a PTC solution for multi-port hub configuration. For single port configurations, see Figures 7 and 8 elsewhere in this document.



**Fig. 2: USB 3.0 multi-port hub configuration (see also Figs. 7 & 8).**

Figure 3 shows the recommended PTC devices for both a single port and two ports in ganged configurations. We have also identified the PTC solution for the new USB Battery Charging specification Rev 1.2.

When selecting a PTC for USB port protection, one needs to consider a few key parameters:

1. Max port current (USB 3.0 is 900mA)
2. Operating temp at the PTC location
3. Trip speed
4. DC Resistance

The PTCs in Figure 3 were selected for their optimal fit for USB 3.0 port protection. All the PTCs are capable of holding the maximum USB 3.0 port current of 900mA per port without tripping at the maximum operating temperature of 60°C. PTCs de-rate due to temperature dramatically so this is an important aspect of the PTC selection process. Designers should also consider the effects of non-compliant USB 3.0 devices that draw more than 900mA when selecting the PTC. The hold current at the maximum operating temperature needs to be greater than the maximum available current if drawing more than 900mA. Otherwise, the PTC has the possibility of nuisance tripping the port.

Each PTC is capable of tripping in less than 5 seconds for an 8A short circuit fault. This is important in meeting the UL60950-1 Limited Power Source specification as well as the 5A current limit in the USB 3.0 Specification.

The last remaining critical parameter in selecting the optimal PTC is DC resistance. Because USB 3.0 is now providing a maximum of 900mA current, power dissipation in the circuit becomes critical and needs to be minimized. Also, the voltage drop across the components on Vbus needs to be minimized especially if the circuit has a tight resistance budget. The PTCs shown in Figure 3 all are made of the Lo-Rho resistivity PTC formulation and are optimal for the USB 3.0 application.

The main objective in selecting a PTC is ensuring that the hold current for the device is at least 900mA at design temperature. We have selected 60°C as the worst case for the products shown in Figure 3. For 1-port applications, the optimal choice is part number 0603L150SLYR because it offers the smallest form-factor available that can still support the required amount of current (0.95A) at the max. design temperature of 60°C.

For situations where the design requires more margin on hold current, part number 1210L200SLYR is a good choice because it holds 1.29A at 60°C. For 2-port applications where the designer can gang two ports together (total 1.8A output) and use one PTC to protect both ports, part number 1206L350SLYR is a good choice because it can hold 2.19A at 60°C. All the suggested parts are capable of tripping in less than 5 seconds at 8A fault current so all safety considerations are met.

Number of USB 3.0 Ports	Littelfuse P/N	Footprint	Vmax (Vdc)	Ihold 20°C (A)	Ihold 60°C (A)	8A trip (sec), 20°C	R1max (Ω)
1	0603L150SLYR	0603	6	1.5	0.95	0.5	0.08
1	1210L200SLYR	1210	6	2	1.29	3	0.024
2	1206L350SLYR	1206	6	3.5	2.19	5	0.018
Battery Charging 1.2 (1 port)	1206L260SLTHYR	1206	6	2.6	1.65	4	0.026

**Fig. 3: Littelfuse PTC products recommended for USB 3.0.**

## Electrostatic Discharge (ESD) Protection

The additional data pairs of USB 3.0 expose systems to greater ESD threats because it provides more possible entryways for the electrical transients.

Interfaces such as USB 3.0 can be exposed to ESD by a number of mechanisms, including the user touching any of the pins on the connector or any of the pins on an open-ended cable connected to one of the ports. Even though modern IC chips often have some degree of protection (usually between 500V to 2kV), these ESD levels are based on the MIL-STD HBM model with a 1500Ω discharge resistor. With the MIL-STD model, a 2kV pulse is closer to the IEC 61000-4-2 model at 500V, which uses a 330Ω discharge resistor. The current available in the HBM pulse is about one-quarter that available from the IEC model at the same transient voltage.

ESD events often can reach 15kV or more and cause soft failures, latent damage or catastrophic failure. Supplemental ESD protection is needed to enhance the survivability of today's modern interface ports. To determine the immunity of systems to external ESD events, several test standards have been developed, with the International Electrotechnical Commission (IEC) 61000-4-2 being the most widely recognized. This standard defines ESD test levels that relate to different environmental and installation conditions and establishes test procedures. Today's SuperSpeed USB 3.0 ports must be able to survive a direct contact ESD of at least 8 kV, which is also an IEC 61000-4-2 level 4 requirement.

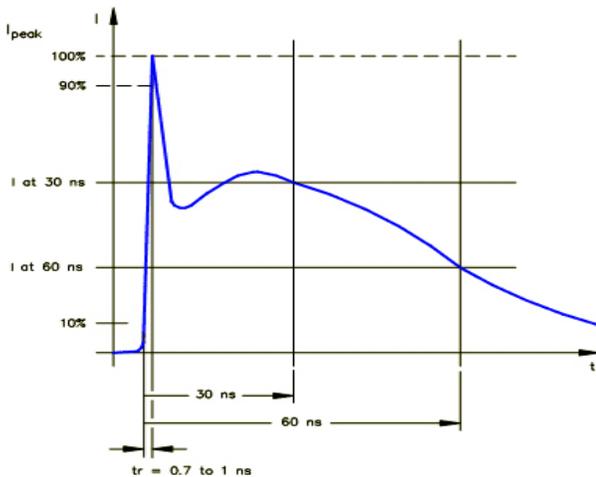


Fig. 4: IEC 61000-4-2 ESD current waveform.

With the higher data rates, particular attention needs to be paid to the capacitance of the components selected to protect the circuitry, but there are many other important parameters system designers should be aware of when selecting an ESD protection device. These include:

- Dynamic resistance and clamping voltage
- Breakdown voltage
- Parasitic capacitance
- Maximum ESD capability
- Multiple pulse capability
- Package geometry
- Off- state impedance or leakage current
- Device configuration and layout flexibility

Several different ESD suppression technologies such as MLVs (Multi-layer varistors), polymer ESD suppressors and silicon-based devices are available on the market today and selecting the right protection will determine whether a USB 3.0 port will survive an ESD event or not.

Designers must be especially mindful of device capacitance, clamping voltage and dynamic resistance because these parameters are critical in selecting the best ESD protection. Some protection device manufacturers have designed their products for a minimal parasitic capacitance to maximize signal integrity while others have maximized clamping performance at the cost of higher capacitance.

Silicon-based devices such as TVS Diodes and Diode Arrays with the lowest dynamic resistance, offer superior clamping performance and have been able to maintain very low parasitic package capacitance. Figure 5 illustrates the clamping performance of silicon vs. MLV ESD protection technologies. As can be seen, silicon-based solutions offer the lowest clamping voltage.

The USB 3.0 eye diagram test results in Figure 9 illustrate how Littelfuse TVS Diode Arrays offer the best technology for protecting USB 3.0 applications against ESD by combining low clamping and low capacitance.

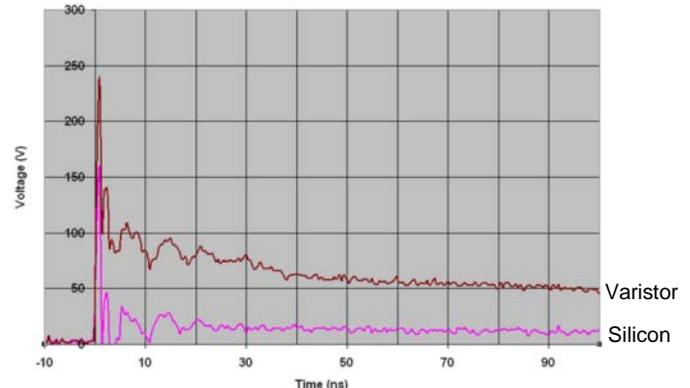


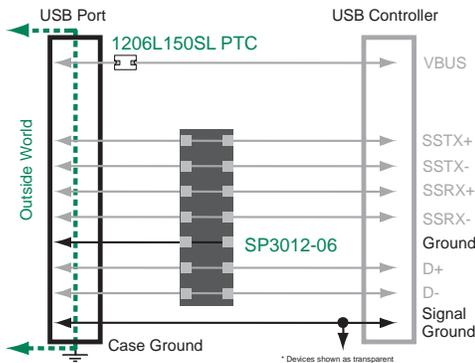
Fig. 5: Clamping performance of silicon versus varistor.

TVS Diode Array devices such as the Littelfuse SP3012-06UTG offer a multi-channel ESD protection solution that's ideal for USB 3.0 protection. Littelfuse SPA® devices work in two ways. First, they absorb the transient with diodes, to steer the current, and second, an avalanche or zener diode clamps the voltage level. Figure 7 depicts a USB 3.0 ESD protection solution using a Littelfuse SP3012-06UTG.



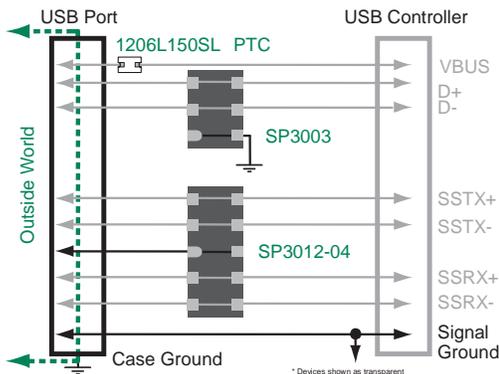
**Fig. 6: Littelfuse SP3012-04UTG and SP3012-06UTG TVS Diode Arrays were specifically designed for USB 3.0 protection.**

Offering six lines of  $\pm 12\text{kV}$  ESD protection, and being able to protect all USB 3.0 data lines in a single 3.5x1.35mm package, the Littelfuse SP3012-06UTG allows designers to stop worrying about using multiple ESD protection devices, which take up valuable board space. Furthermore, the SP3012 has an extremely low dynamic resistance of only  $0.4\Omega$ . This provides best-in-class clamping performance for USB 3.0 chipsets or transceiver ICs that are very sensitive to overvoltage events.



**Fig. 7: USB 3.0 ESD protection with SP3012 device.**

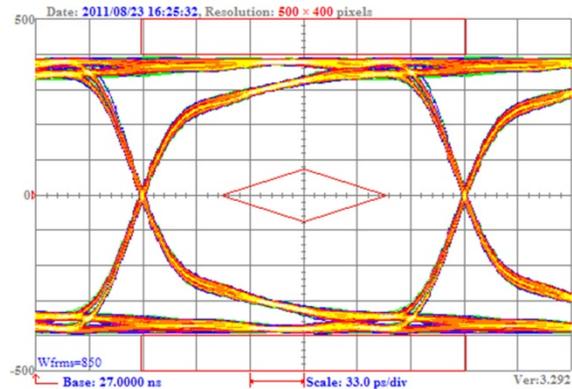
Alternatively, for designers who prefer to implement a two-device solution, the SP3012-04UTG and SP3003-02UTG are recommended for protecting the six data lines (see Figure 8). The SP3003 protects the legacy D+/D- pair while the SP3012 protects the two SuperSpeed differential pairs.



**Fig. 8: USB 3.0 ESD protection with SP3012 and SP3003.**

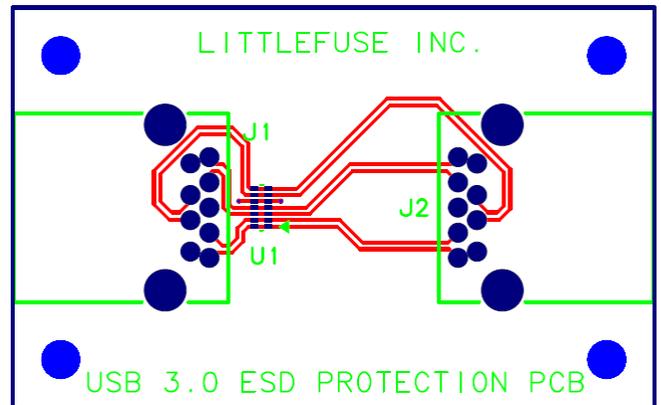
## Signal Integrity

Maintaining USB 3.0 data integrity is critical and any small amount of added capacitance can cause signal distortion and degrade signal reliability. One way to characterize the effect that an ESD suppressor's parasitic capacitance will have on signal integrity is to conduct eye diagram testing. This test involves repetitively sampling a digital signal and displaying the resulting eye pattern on an oscilloscope. A mask is often used to define acceptable signal qualities and compliance.



**Fig. 9: Eye diagram of SP3012 Series at 5Gbps.**

Figure 9 displays a "passing" eye diagram of the Littelfuse SP3012-06UTG using a 5Gbps USB 3.0 compliance test pattern and mask; Figure 10 shows the PCB layout of the evaluation board. In order to simulate a real world USB 3.0 data path, test boards were designed with  $90\Omega$  differential signal pairs and USB 3.0 connectors.



**Fig. 10: Snapshot of the SP3012-06UTG evaluation board.**

It can be seen that signals are well within mask boundaries and wide eye width is maintained, offering designers flexibility within a system's capacitance budget.

**Littelfuse, Inc.**  
8755 West Higgins Road, Suite 500  
Chicago, IL 60631 USA  
Phone: (773) 628-1000 [www.littelfuse.com](http://www.littelfuse.com)