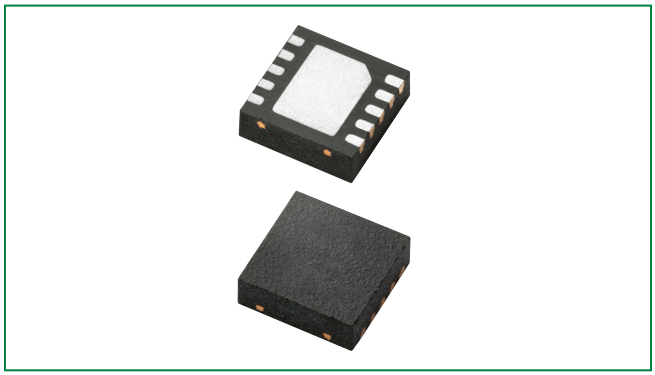
LS0502SCD33

Super Capacitor Protection IC for Backup Power Applications



Features and Benefits

- 2.5 V to 5.5 V System Voltage
- 18 V Input Rating with Overvoltage Protection
- Programmable 1.1 V to 5.3 V Cap Voltage Range
- Programmable Super Capacitor Charge Current
- Programmable Input Overcurrent Protection
- Automatic Cell Balancing
- Automatic Main/Backup Switchover
- Up to 2 A Discharge Current
- Programmable Voltage and Current Thresholds
- ±2 % Threshold Accuracy
- 2.5 µA Ready Quiescent Current
- Small Solution Size
- DFN Package

Description

The LS0502SCD33 is a complete solution for system with backup storage capacitor or capacitor bank. It integrated input overvoltage, overcurrent protection circuit, a reverse blocking switch and super capacitor charging control circuit. It also has built-in cell balance to provide protection over two cell super capacitor system.

When the main supply is present and above the minimum system supply voltage, system will draw power from input supply. At the same time, integrated linear charger charges the storage element at up to 300 mA current. Once the storage element is charged, the circuit draws only 2.5 µA of current while it maintains the super capacitor or other storage element in its ready state. When the main supply is removed, the integrated reverse blocking switch will block current flow from system rail to input. The linear charger will be turned on to provide power to system rail with low resistance path with up to 2 A current.

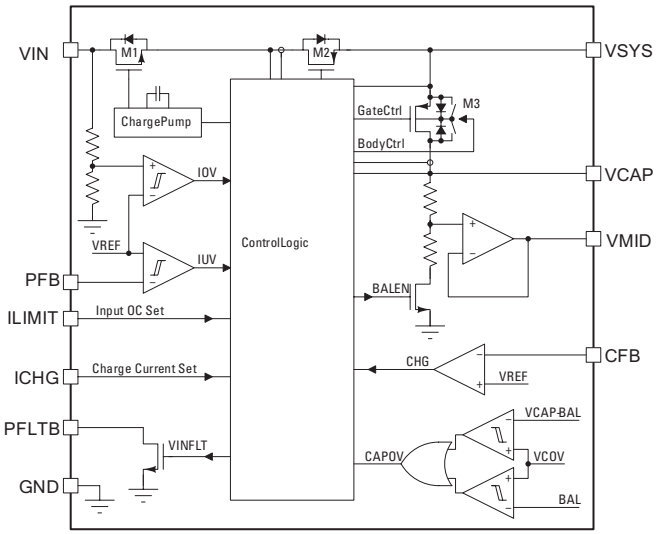
Integrated cell balancing circuit will keep monitoring the cell voltage when charging and keep the two cells voltage at same level.

The LS0502SCD33 is externally programmable for input current limit, input overvoltage, charge current limit, and charge voltage limit. It provides a flag signal when input supply is unplugged so that main system can taking action.LS0502SCD33 is available in DFN3X3-10 package.

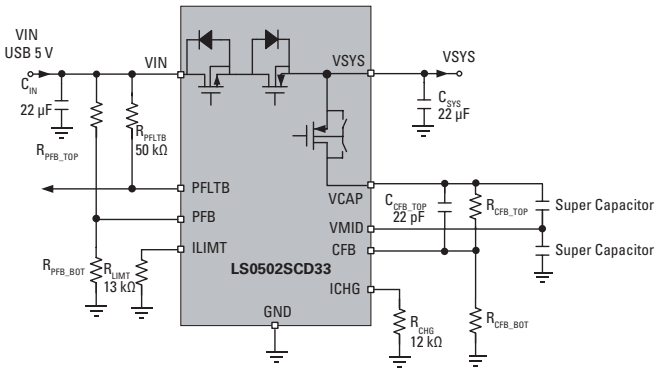
Applications

- Handheld Industrial Equipment
- Dash Camera
- IoT
- SmartMeter
- Portable Device with Removable Battery

Functional Block Diagram



Typical Applications



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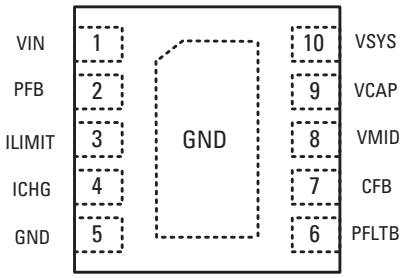
Pinout Designation



Exposed Pad on Backside

Pin #	Pin Name	Description
1	VIN	Input Power Supply. Connect to a 5 V system supply rail and bypass with a 10 µF capacitor to GND.
2	PFB	Input voltage sensing input. Connect to the center point of a resistor divider from VIN to GND. It is compared with internal 1.2 V reference. When PFB is below1.2 V, PFLTB will pull high to indicate input power failure."
3	ILIMT	Input overcurrent protection setting pin. Connect a resistor to ground the set the input overcurrent protection level. If ILIMT is short to GND, input current limit is set to 3 A. If ILIMT is floating, input current limit is 0 A. The Limit current is determined by the equation: ILIMT = 30 A*kΩ/RLIMIT
4	ICHG	Charge Current Input. This pin sets the maximum current level for charging super capacitor. The charger current recommend <350 mA (R_{CHG}>10 k). The Charge Current is determined by the equation: ICHG = 3.3 A*kΩ/R_{CHG}
5	GND	Ground.
6	PFLTB	Open-Drain input power failure indicator. PFLTB goes low when the PFB drop below 1.2 V or (VIN-VSYS) exceed 360 mV. Connect to an external pull up resistor.
7	CFB	VCAP Feedback. Connect to the upper point of a resistor divider from VCAP to GND. Part stops charging super capacitor when CFB voltage is above 1.1 V.
8	VMID	Super capacitor balance point. Connect to center point of stacked two super capacitors.
9	VCAP	Super Cap. Connect to top point of two super cap stacks.
10	VSYS	Supply rail for internal system. Power is draw from VIN when valid input supply is present. When input power failed, power will be provided by super capacitor connected to VCAP.
EP	EP	Note: EP use conductive glue and GND PAD has no down bonding.

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Absolute Maximum Rating (Reference to GND)

Symbol	Value	Units
VCAP, VSYS, PFLTB to GND	-0.3 to +6	V
VIN to GND	-0.3 to +18	V
VMID, CFB to GND	-0.3 to VCAP+0.3	V
PFB, ILIMT, ICHG to GND	-0.3 to VSYS+0.3	V
ESD	Class 2	-
Lead Temperature (Soldering 10 s)	260	°C
Junction Temperature Range	-40 to +150	°C
Storage Temperature Range	-65 to +150	°C

* Notes:Stress exceeding those listed "Absolute Maximum Ratings" may damage the device.

Thermal information

Symbol	Value	Units
Maximum Power Dissipation (T_A = 25 °C)	2.3	W
Thermal Resistance (θ_{JA})	53	°C/W
Thermal Resistance (θ_{JC})	25	°C/W

Note1: Measured on JESD51-7, 4-Layer PCB.

Note 2: The maximum allowable power dissipation is a function of the maximum junction temperature T_{J_MAX}, the junction to ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\_MAX} = (T_{J\_MAX}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Recommend Operating Conditions

Symbol	Value	Units
Input Voltage (VIN)	+4.0 to +5	V
Cap Voltage (VCAP)	+0.8 to +5.4	V
Operating Temperature Range	-40 to +85	°C
Junction Temperature Range	-40 to +125	°C

* Notes: The device is not guaranteed to function outside of the recommended operating conditions.

Electrical Characteristics (T_A = +25 °C, VIN = 5 V, VCAP = 5 V, unless otherwise specified) Note 1

Parameter	Test Conditions	Min	Typ	Max	Unit
Input Voltage Range		2.5		5.5	V
VSYS Charging Supply Current	PFB>1.2 V, VIN = 5 V		650		µA
VSYS Backup Supply Current	PFB = 0, VCAP = 5 V		1.5		µA
VCAP UVLO Threshold	VCAP falling	1.45	1.65	1.85	V
VCAP UVLO Hysteresis			200		mV
INPUT OVP OCP Switch					
Input Overvoltage Protection Threshold voltage	VIN Rising		6.0		V
Input Overvoltage Hysteresis			0.4		V
Input Overcurrent level	R_{ILIMT} = 25.5 kΩ		1.2		A
Max Input Overcurrent Level	VIN>4.2 V,ILIMT connect to GND		2.7		A
Input Overvoltage Switch Rdson			0.1		Ω
Ideal Diode					
Drain Source regulation voltage			25		mV
Source Drain fast reverse blocking threshold voltage (Note 2)			-20		mV
PMOS Rdson			50		mΩ
PMOS Leakage Current				0.1	µA

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Electrical Characteristics (T_A = +25 °C, VIN = 5 V, VCAP = 5 V, unless otherwise specified) Note 1

Parameter	Test Conditions	Min	Typ	Max	Unit
Super Capacitor Charger/Discharger					
V_{CFB} Threshold Voltage to Stop Charging		1.04	1.08	1.12	V
V_{CFB} Hysteresis			40		mV
CFB Regulation Reference Voltage		1.05	1.1	1.15	V
CFB Leakage Current				50	nA
Charge Current	R_{ICHG} = 33 kΩ, VCAP = 3 V	75	100	125	mA
	R_{ICHG} = 33 kΩ, VCAP = 0 V	30	45	60	mA
Charging/Discharging PMOS Rdson			100		mΩ
Capacitor Voltage Clamp for each Capacitor		2.44	2.65	2.76	V
Maximum Capacitor Stack Voltage		4.88	5.3	5.52	V
VMID Balance Source Current Threshold	VCAP = 4 V, VMID Rising	1.93	1.99	2.04	V
	VCAP = 4 V, VMID Falling	1.92	1.98	2.03	V
VMID Balance Sink Current Threshold	VCAP = 4 V, VMID Rising	1.96	2.02	2.07	V
	VCAP = 4 V, VMID Falling	1.95	2.01	2.06	V
PMOS Body Diode Switch (VCAP-VSYS) Threshold Voltage	VCAP ramp up from below VSYS		100		mV
PMOS Charge Mode and Switch Body V_{DS} Threshold Voltage	VCAP ramp down from above VSYS		250		mV
VCAP Charge Mode Threshold (VSYS- VCAP) Voltage	VCAP ramp down from above VSYS		10		mV
VCAP Charge Threshold (VSYS- VCAP) Hysteresis Voltage	VCAP ramp up from below VSYS		-100		mV
Input Power Fail Comparator					
V_{PFB} Threshold Voltage (Falling)			1.2		V
V_{PFB} Hysteresis			85		mV
VSYS Power Good Threshold	VIN -VSYS		260		mV
VSYS Power Fail Threshold	VIN-VSYS		320		mV
PFLT Output Low Voltage	I_{SINK} = 1 mA		100		mV
PFLT High Impedance Leakage	V_{PFLT} = 5 V			0.1	µA
PFLT Deglitch Time			3.5		ms
Thermal Shutdown Temperature	T_J rising, 30 °C typical hysteresis		150		°C
Thermal Shutdown Hysteresis			30		°C

Note 1: Limits are 100 % production testes @ T_A = +25 °C, unless otherwise noted. Limits over the temperature range are guaranteed by design.

Note 2: Guaranteed by design, not production tested.

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Typical Performance Characteristics C_{IN} = 22 µF, C_{SYS} = 22 µF, R_{LIMT} = 13 kΩ, R_{CHG} = 12 kΩ, T_A = +25 °C)

Fig1 : Charger Current vs. VCAP Voltage

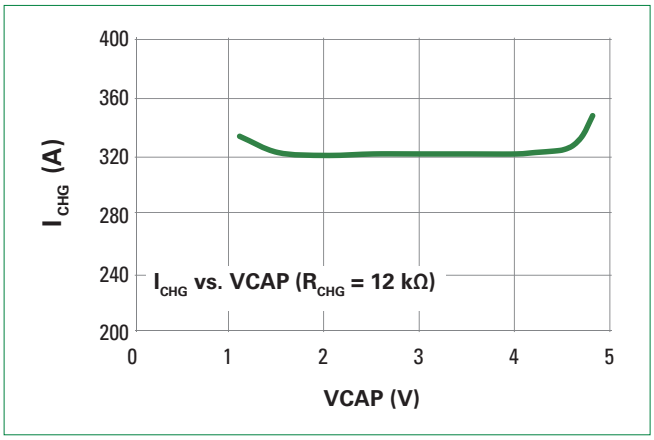

Fig2 : Charger Current vs. VCAP Voltage

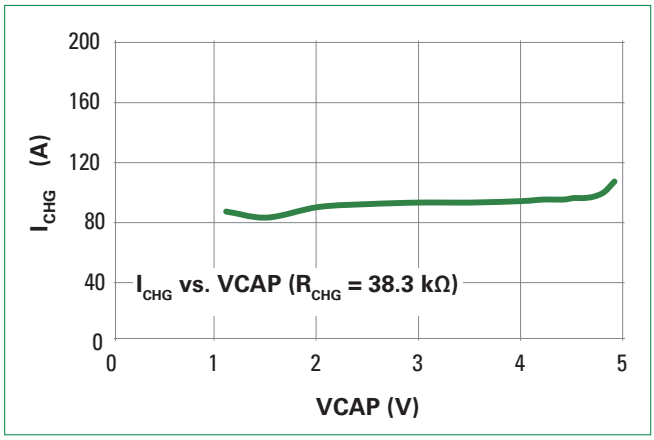

Fig3 : Charger VIN Power on

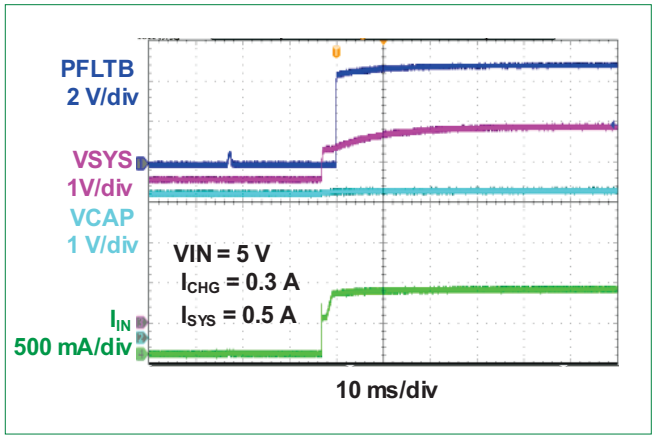

Fig4 : Charger VIN Power off

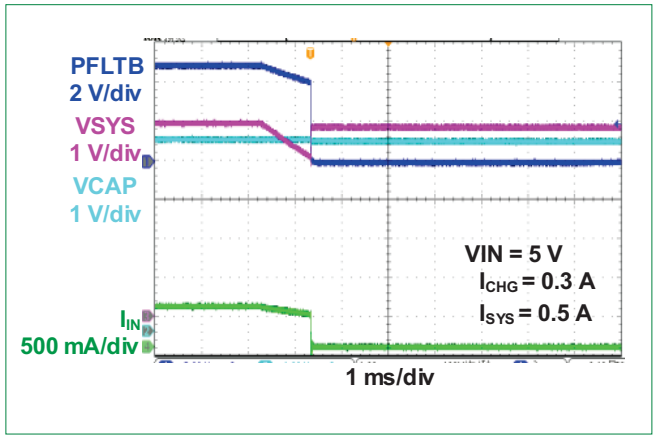

Fig5 : Charging Time (SuperCap1 = SuperCap2 = 20 F)

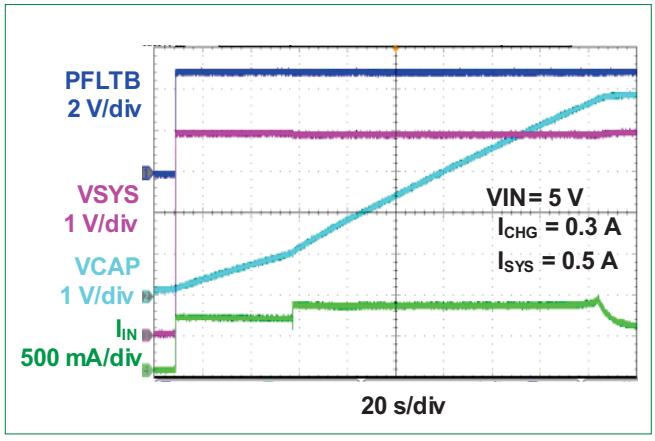

Fig6 : Discharger Time (SuperCap1 = SuperCap2 = 20 F)

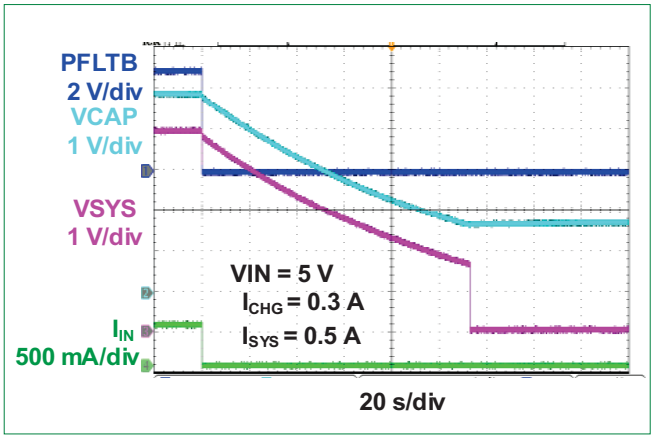

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Fig7 : Charger Mode VCAP Short

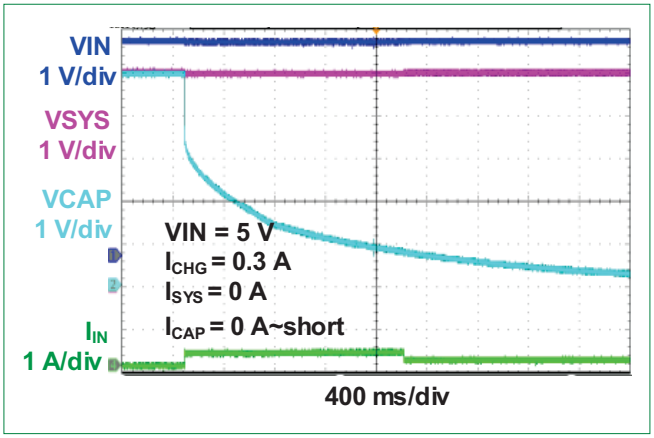

Fig8 : Charger TC Mode -> CC Mode

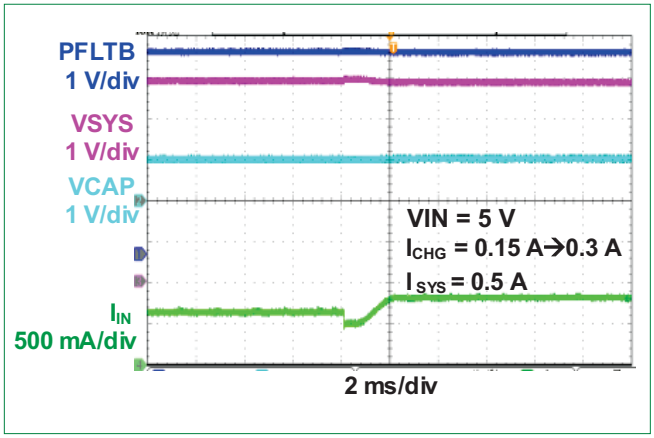

Fig9 : Charger 4VIN Switch to 5VIN

(Setting VIN_UVLO 4.1 V)

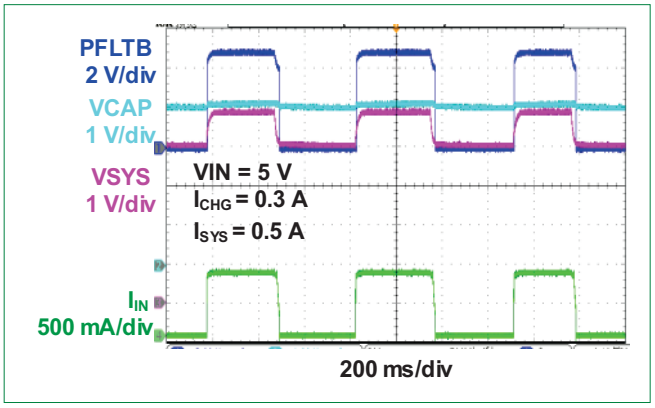

Fig10 : VIN OVP Protection

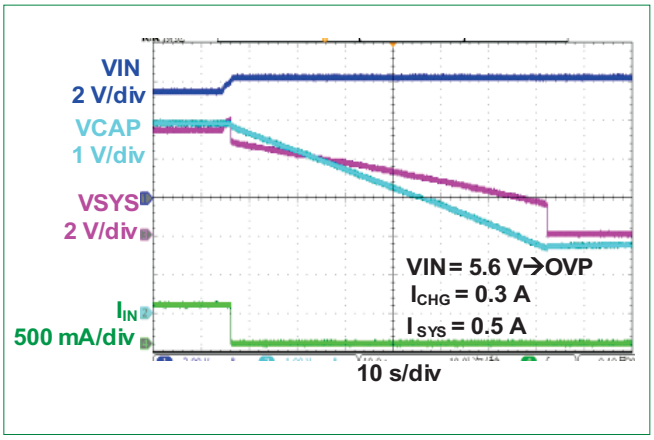

Fig11 : VIN OVP Recovery

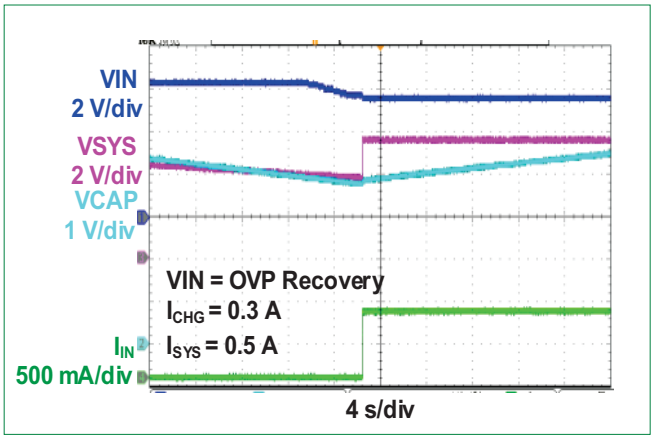

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Fig12 : Charger Mode VSYS Short

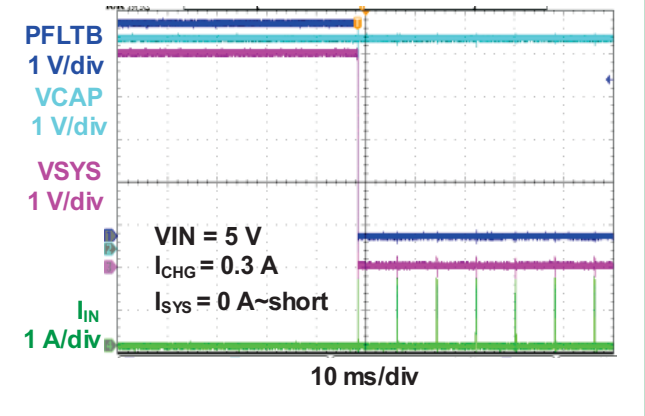


Fig13 : Charger Mode VSYS Short Recovery

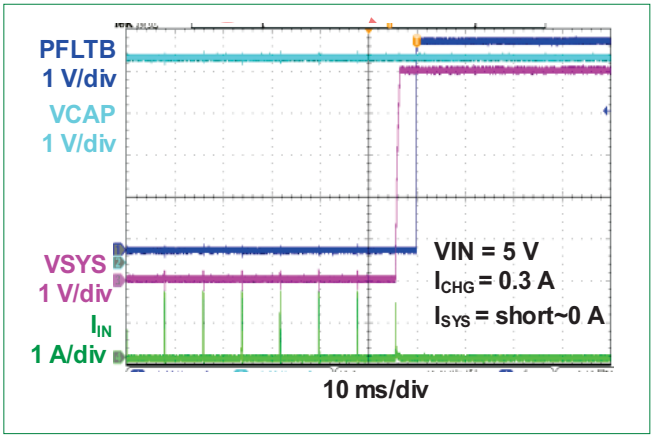


Fig14 : Discharger Mode VSYS Short

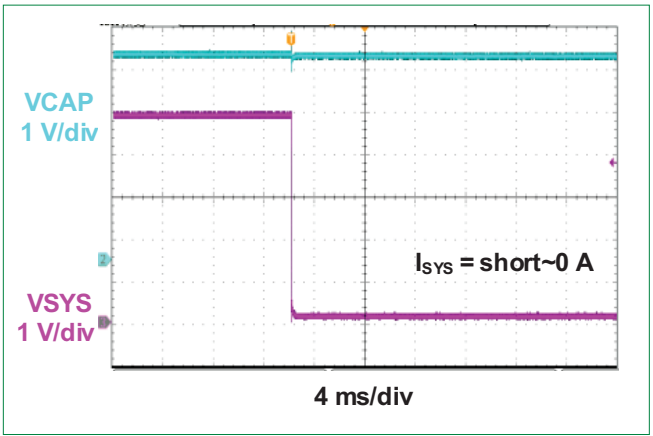
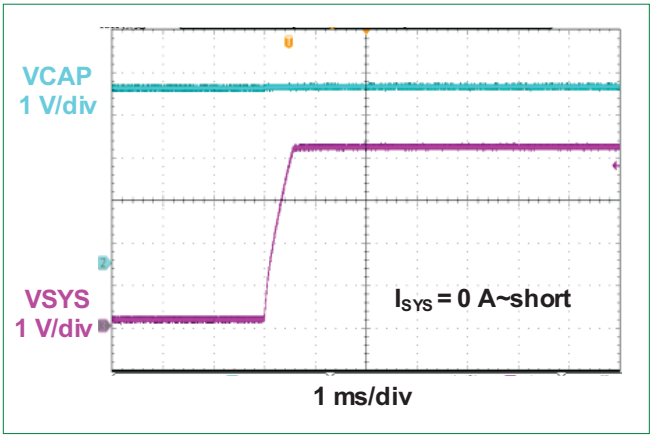


Fig15 : Discharger Mode VSYS Short Recovery



Description

For applications which require backup power in harsh environment, Lithium-Ion battery cannot be used due to limited temperature range. Super capacitor with wide operating temperature range and high power/energy density, provides a safe and compact solution. For many systems, the high operating voltage (>3 V) requires a power management system for super capacitor with two stacked cells or use a BOOST converter with inductor. Many systems also require long standby time (weeks of time), this need can only be realized with very low quiescent current.

LS0502SCD33 provides a flexible, integrated and compact storage capacitor or capacitor bank backup solution with extensive protection function to ensure a safe, efficient, compact and low cost solution for these applications. LS0502SCD33 integrates input overvoltage/ current protection to prevent damage to following system. It also integrates an ideal diode for reverse blocking when input voltage is lost.

LS0502SCD33 integrates a linear charger to charge super capacitor with as high as 350 mA current to achieve fast and safe charging. The charging devices also act as power path control switch. When input power is lost, this switch can be turned on to keep the system rail stable in backup mode. In backup mode, quiescent current draw from super capacitor is only 2.5 µA. This ensures very long standby time of the system with low capacitance super capacitor.

LS0502SCD33 integrates a programmable Input voltage monitor. When input voltage drops below certain voltage set by resistor divider connected to PFB pin, a flag signal on PFLTB will inform the following system about the event so that preventative actions can be taken like process and save data in DRAM. With 2 super capacitors in stack, LS0502SCD33 integrates cell balancing function. During charging mode, voltage between two stack capacitor is compared with half of total capacitor voltage. Current is diverted to keep these two voltages close to each other. LS0502SCD33 also integrates cell monitoring and protection circuit. This circuit monitors voltage for each capacitor. During charging mode, if any capacitor voltage reaches 2.65 V, charging will be stopped until this fault is gone. Same way, during discharge mode, if any of the capacitor voltage drop below ground, discharging will be stopped to protect the capacitors.

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OPERATION

The system should have three states: STANDBY State, CHARGE State, DISCHARGE State and UVLO State.

STANDBY State:

1.VCAP > VSYS, VIN is still available and PFB higher than threshold voltage. Or,

2.VCAP reaches setting point by CFB and VIN is still available and PFB higher than threshold. Or,

3.Any of the two super capacitor voltage reaches internal protection point and VIN is still available.

In STANDBY State, M3 FET should be kept OFF. M3 body diode need to be switches according to VSYS VCAP voltage.

CHARGE State:

VSYS > VCAP, VIN is available and healthy; VCAP is below setting point by CFB. Both super capacitors are below overvoltage protection point. In this state, we will turn of M3 with current limit set by ICHG.

Two possible features need to be evaluated:

1. Input DPPM. If input voltage drop and PFB voltage drops close to set point, we can fold back charge current to limit current drain from weak input source

2. Soft charging ending. When VCAP is charged and CFB voltage getting close to set point, we can fold back charge current so that when charge stops, voltage drop on any impedance in series with capacitor doesn't cause oscillation between charge mode/standby mode.

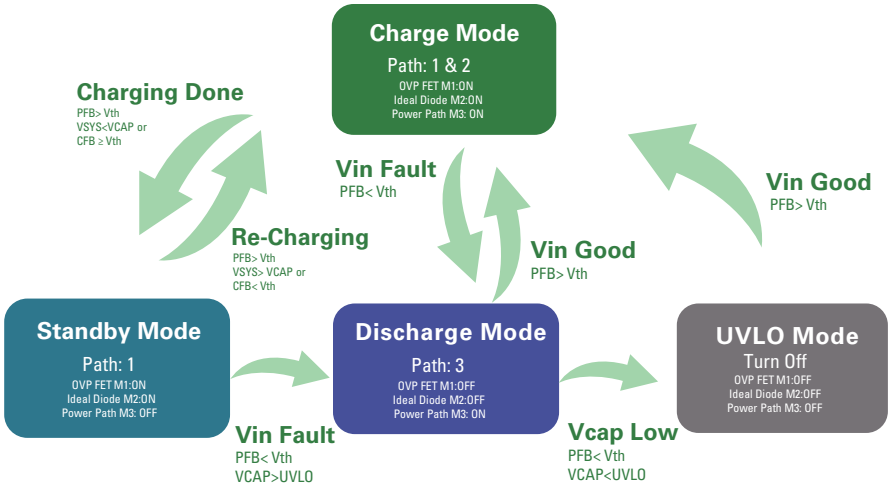
DISCHARGE State:

When PFB is below threshold, we consider input power source is gone. In this case, OVP FET is turned off. Ideal diode should be turned off too. Power path control FET M3 is turned on to connect VCAP to VSYS. Transition from Charge Mode or Standby Mode to Discharge Mode need to be smooth without huge inrush current, at the same time, it cannot let VSYS drop too much which might cause downstream system to shut down.

In Discharge mode, all the bias current is supplied by VCAP. To extend operating time, quiescent current need to be below 1 μA in this case. Circuits need to be alive are: 1. M3 overcurrent detection circuit; 2. UVLO detection circuit for VCAP.

UVLO State:

In case the system runs on Super Capacitor for long time without recharge, eventually VCAP will drop too low to sustain the function of the whole system When VCAP drops too low, we will enter UVLO state. In this state, all the circuit is shut down. This state can only be cleared if VIN is supplied.



PCB Layout Guideline

- The high current paths (GND, VIN, VSYS and VCAP) should be placed very close to the IC with short, direct and wide traces.
- Put the input capacitors and VSYS capacitors as close to the VIN/VSYS and GND pins as possible.
- Keep the VIN and GND pads connected with large copper and use at least two layers for IN and GND trace to achieve better thermal performance. Also, add several vias with 10 mil_drill/18 mil_copper_width close to the VIN and GND pads to help on thermal dissipation.
- Four-layer layout is strongly recommended to achieve better thermal performance.

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Soldering Parameters

Average ramp up rate (Tsmin to T_P)		1~2 °C/second, 3 °C/second max
Preheat & Soak	**- Temperature Min ($T_{s(min)}$)**	150 °C
	- Temperature Max ($T_{s(max)}$)	200 °C
	- Time (min to max) (t_s)	60 – 120 seconds
Time maintained above	**- Temperature(T_L)**	217 °C
	- Time(t_L)	60~150 seconds
Peak Temperature (T_P)		See Classification Temp in table 1
Time within 5°C of actual Peak Temperature (t_p)		30 seconds max
Ramp-down Rate		6 °C/second max
Time 25°C to Peak Temperature (T_P)		8 minutes max

Note 1: Tolerance for peak profile Temperature(T_p) is defined as a supplier minimum and a user maximum.

Note 2: Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.

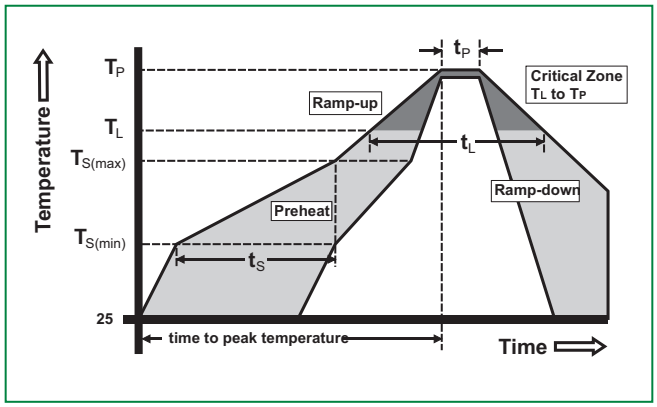


Table 1. Pb-free Process –Classification Temperatures (T_C)

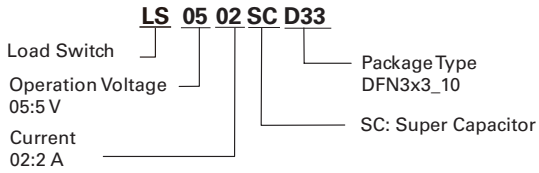
Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm–2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Note: For all temperature information, please refer to topside of the package, measured on the package body surface.

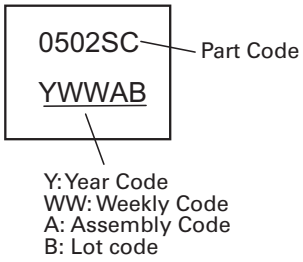
Ordering Information

Part Number	Marking	Package	Min. Order Qty.
LS0502SCD33	0502SC	DFN3x3_10L	5000/Tape & Reel

Part Numbering



Part Marking



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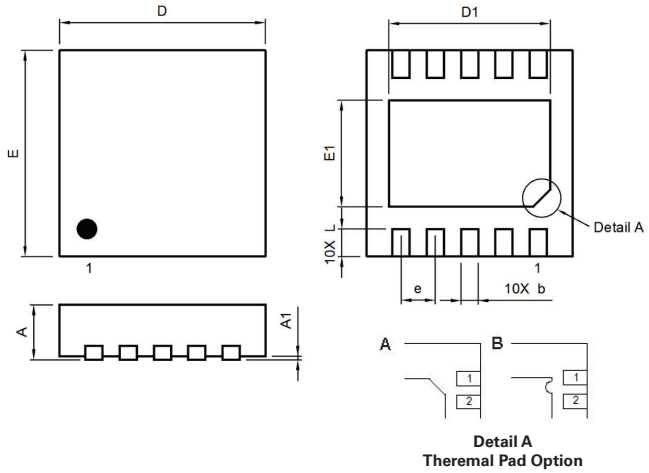
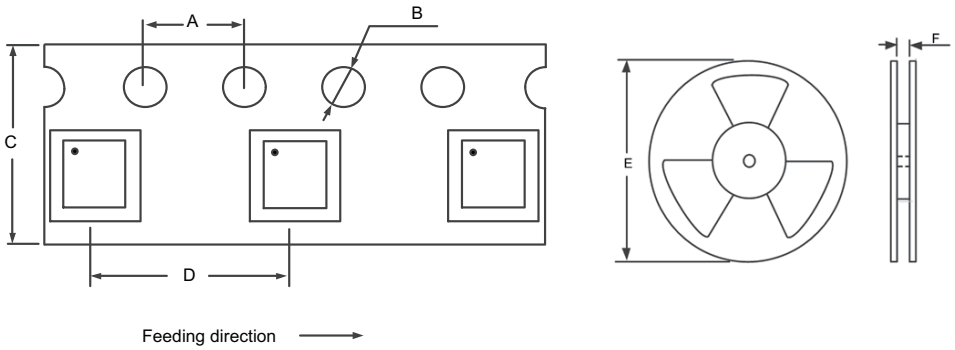
Dimensions — DFN3x3_10L



Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.18	0.30	0.007	0.012
D	2.90	3.10	0.114	0.122
D1	2.10	2.60	0.083	0.102
E	2.90	3.10	0.114	0.122
E1	1.35	1.80	0.053	0.071
e	0.50		0.020	
L	0.30	0.50	0.012	0.020

Carrier Tape & Reel Specification — DFN3x3_10L



Symbol	Millimeters
A	4.0
B	1.5
C	12.0
D	8.0
E	13 inch
F	13.0