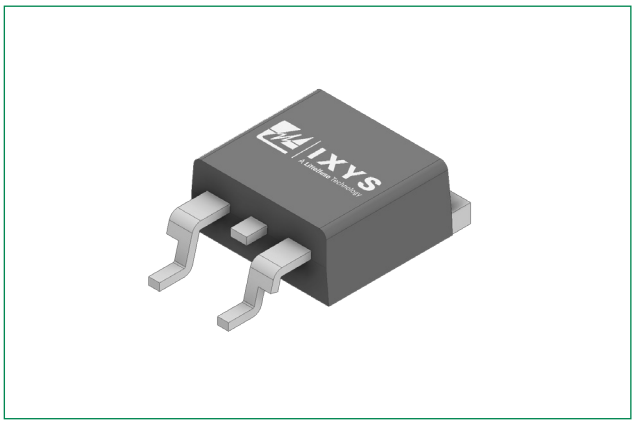
Thyristors
35 Amp Alternistor (High Commutation) Triacs

Q6035NAH5

RoHS



Description

The 35 Amp bi-directional solid state switch series is designed for AC switching and phase control applications such as motor speed and temperature modulation controls, lighting controls, and static switching relays.

Standard type components normally operate in Quadrants I & III triggered from AC line.

Standard alternistor triac components operate with in-phase signals in Quadrants I or III and ONLY unipolar negative gate pulses for Quadrant II or III. The alternistor triac will not operate in Quadrant IV. These are used in circuit applications requiring a high dv/dt capability.

Main Features

Symbol	Value	Unit
$I_{T(RMS)}$	35	A
V_{DRM}/V_{RRM}	600	V
$I_{GT\ (Q1)}$	50	mA

Features & Benefits

- RoHS Compliant
- Glass – passivated junctions
- Voltage capability up to 600V
- AEC-Q101 Qualified
- Surge capability up to 350A at 60 Hz half cycle
- L-Package isolation rating of 2500V rms
- Automotive Level Manufacture Control

Applications

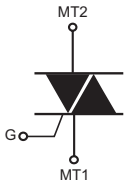
Excellent for AC switching and phase control applications such as heating, lighting, and motor speed controls.

Typical applications are AC solid-state switches, industrial power tools, exercise equipment, white goods and commercial appliances.

Alternistor Triacs (no snubber required) are used in applications with extremely inductive loads requiring highest commutation performance.

Internally constructed isolated packages are offered for ease of heat sinking with highest isolation voltage.

Schematic Symbol



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Absolute Maximum Ratings — Alternistor Triac (3 Quadrants)

Symbol	Parameter			Value	Unit
$I_{T(RMS)}$	RMS on-state current (full sine wave)	Q6035NAH5	T_C = 90°C	35	A
I_{TSM}	Non repetitive surge peak on-state current (full cycle, T_J initial = 25°C)	f = 50 Hz f = 60 Hz	t = 20 ms t = 16.7 ms	290 350	A
I^2t	I^2t Value for fusing	-	t_p = 8.3 ms	508	A^2s
di/dt	Critical rate of rise of on-state current (I_G = 200mA with ≤ 0.1µs rise time)	f = 120 Hz	T_J = 125°C	100	A/µs
I_{GTM}	Peak gate trigger current	t_p=20µs	T_J = 125°C	4	A
$P_{G(AV)}$	Average gate power dissipation		T_J = 125°C	0.5	W
T_{stg}	Storage temperature range			-40 to 125	°C
T_J	Operating junction temperature range			-25 to 125	°C

Electrical Characteristics (T_J = 25°C, unless otherwise specified) — Alternistor Triac (3 Quadrants)

Symbol	Test Conditions	Quadrant		Q6035NAH5	Unit
I_{GT}	V_D = 12V R_L = 30 Ω	I – II – III	MAX.	50	mA
V_{GT}	V_D = 12V R_L = 30 Ω	I – II – III	MAX.	2	V
V_{GD}	$V_D = V_{DRM}$ R_L = 3.3 kΩ T_J = 125°C	I – II – III	MIN.	0.2	V
I_H	I_T = 400mA		MAX.	75	mA
dv/dt	$V_D = V_{DRM}$ Gate Open T_J = 125°C	600V	MIN.	400	V/µs
(dv/dt)c	(di/dt)c = 18.9 A/ms T_J = 125°C		MIN.	20	V/µs
t_{gt}	35A device $I_G = 2 \times I_{GT}$ PW = 15µs I_T = 49.5A(pk)	I – II III	TYP.	3 11	µs

Note: xx = voltage/10

Static Characteristics

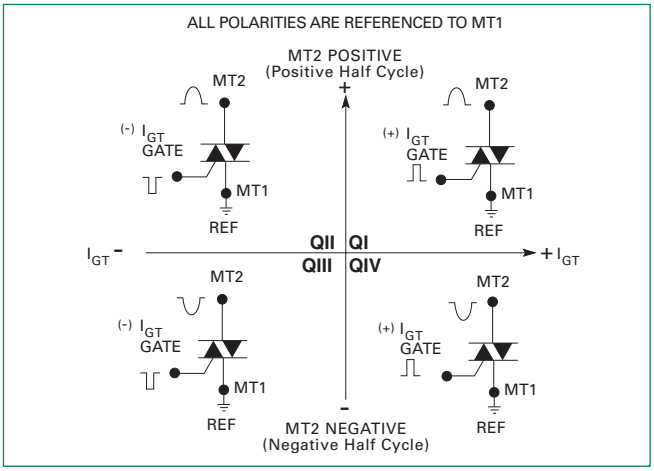
Symbol	Test Conditions					Value	Unit
V_{TM}	35A device I_{TM} = 49.5A t_p = 380 µs				MAX.	1.5	V
I_{DRM} I_{RRM}	$V_D = V_{DRM} / V_{RRM}$	Q6035NAH5	T_J = 25°C T_J = 125°C	600V 600V	MAX.	10 2	µA mA

Thermal Resistances

Symbol	Parameter		Value	Unit
$R_{\theta(J-C)}$	Junction to case (AC)	Q6035NAH5	0.85	°C/W

Note: xx = voltage/10

Figure 1: Definition of Quadrants



Note: Alternistors will not operate in QIV

Figure 2: Normalized DC Gate Trigger Current for All Quadrants vs. Junction Temperature

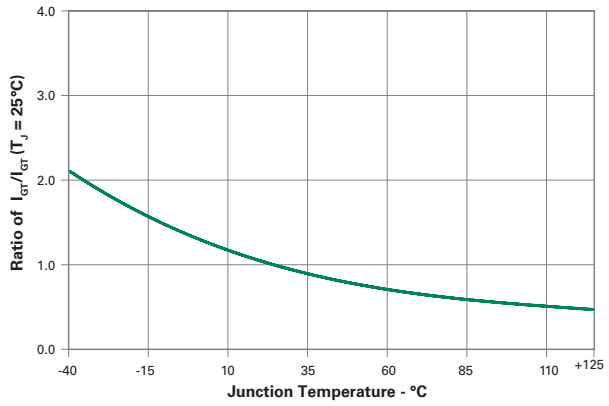


Figure 3: Normalized DC Holding Current vs. Junction Temperature

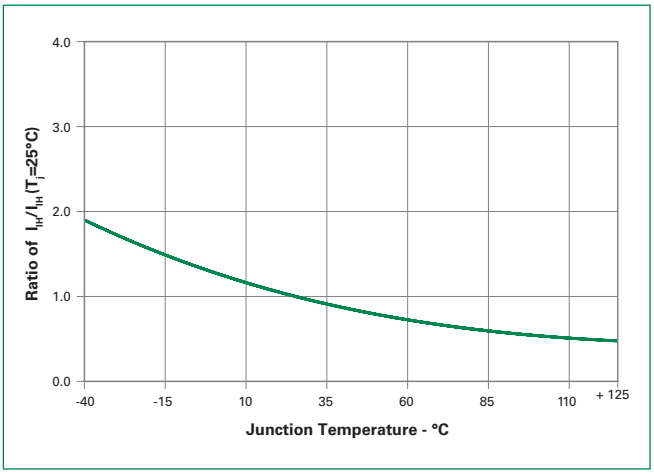


Figure 4: Normalized DC Gate Trigger Voltage for All Quadrants vs. Junction Temperature

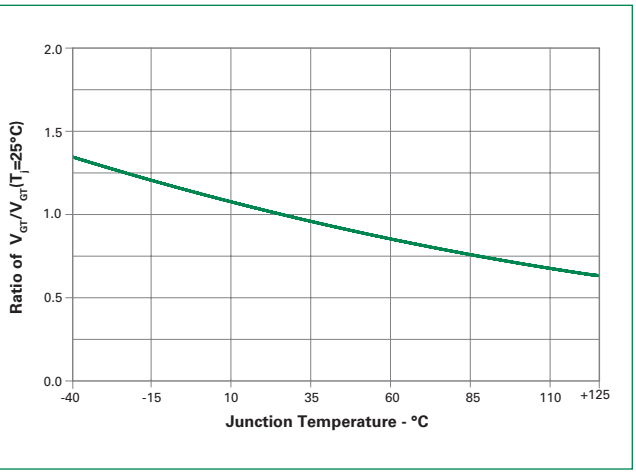


Figure 5: Power Dissipation (Typical) vs. RMS On-State Current

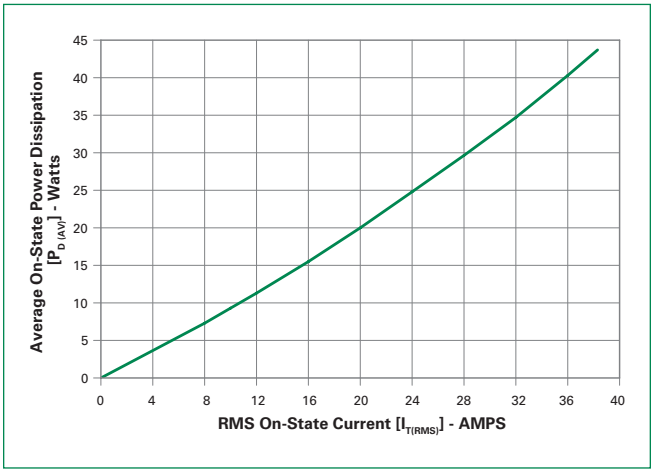
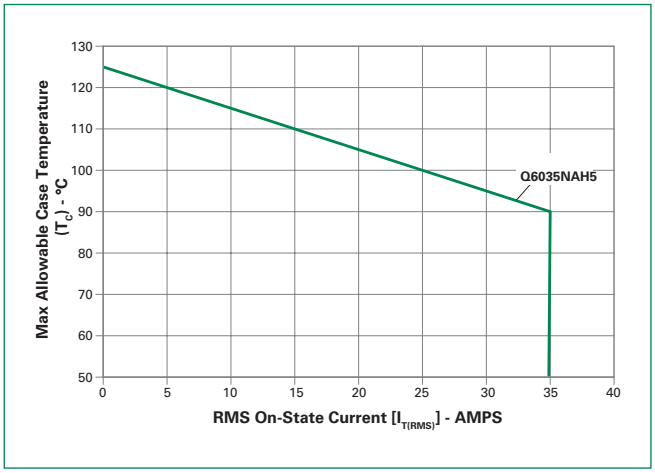


Figure 6: Maximum Allowable Case Temperature vs. On-State Current



Note: xx = voltage

Figure 7: On-State Current vs. On-State Voltage (Typical)

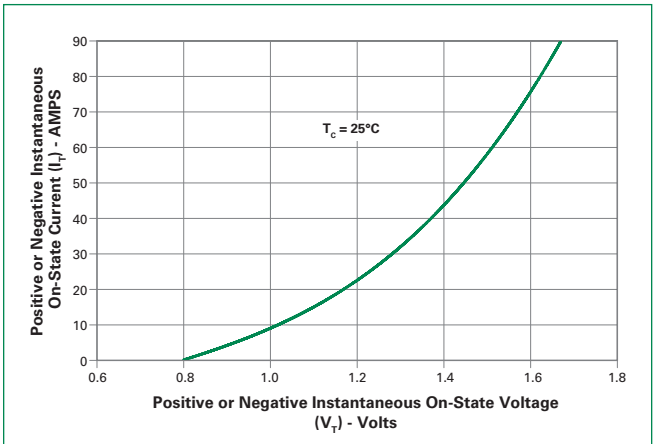
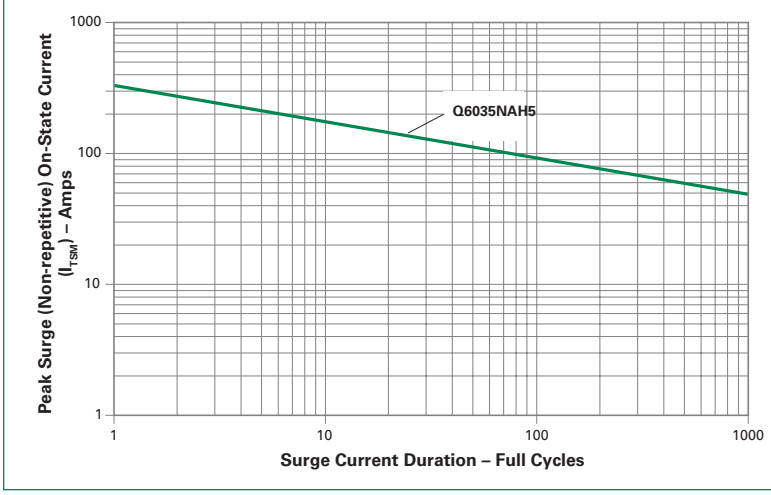


Figure 8: Surge Peak On-State Current vs. Number of Cycles



Supply Frequency: 60Hz Sinusoidal
Load: Resistive
RMS On-State [$I_{T(RMS)}$]: Max Rated Value at Specific Case Temperature

Notes:
1) Gate control may be lost during and immediately following surge current interval.
2) Overload may not be repeated until junction temperature has returned to steady-state rated value.

Note: xx = voltage

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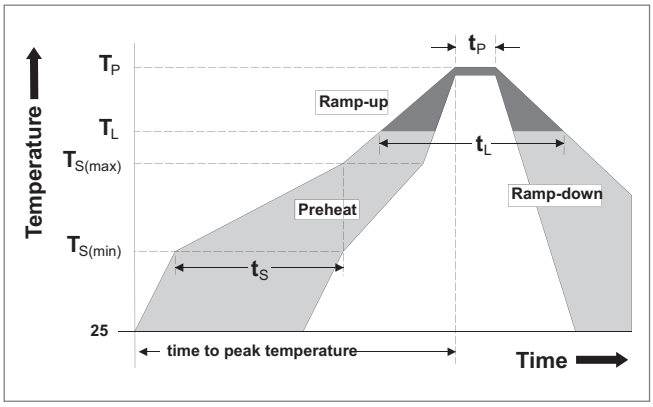
Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	**- Temperature Min ($T_{s(min)}$)**	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus Temp) (T_L) to peak		5°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		5°C/second max
Reflow	**- Temperature (T_L) (Liquidus)**	217°C
	- Time (min to max) (t_s)	60 – 150 seconds
Peak Temperature (T_p)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		5°C/second max
Time 25°C to peak Temperature (T_p)		8 minutes Max.
Do not exceed		280°C



Physical Specifications

Terminal Finish	100% Matte Tin-plated.
Body Material	UL Recognized compound meeting flammability rating V-0
Terminal Material	Copper Alloy

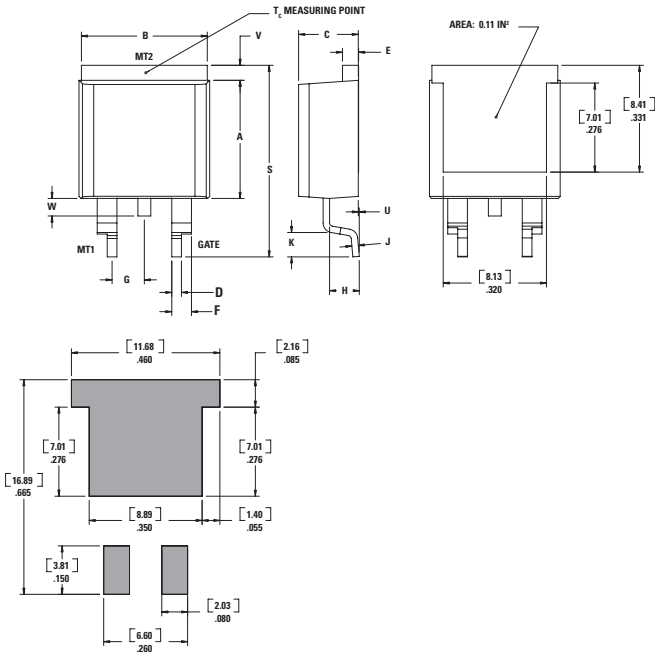
Environmental Specifications

Test	Specifications and Conditions
AC Blocking	MIL-STD-750, M-1040, Cond A Applied Peak AC voltage @ 125°C for 1008 hours
Temperature Cycling	MIL-STD-750, M-1051, 1000 cycles; -40°C to +150°C; 15-min dwell-time
Temperature/Humidity	EIA / JEDEC, JESD22-A101 1008 hours; 320V - DC: 85°C; 85% rel humidity
UHAST	JESD22A-118, 96 hrs, 130°C/ 85% RH
Resistance to Solder Heat	MIL-STD-750 Method 2031
Solderability	ANSI/J-STD-002, category 3, Test A
Lead Bend	MIL-STD-750, M-2036 Cond E

Design Considerations

Careful selection of the correct component for the application's operating parameters and environment will go a long way toward extending the operating life of the Thyristor. Good design practice should limit the maximum continuous current through the main terminals to 75% of the component rating. Other ways to ensure long life for a power discrete semiconductor are proper heat sinking and selection of voltage ratings for worst case conditions. Overheating, overvoltage (including dv/dt), and surge currents are the main killers of semiconductors. Correct mounting, soldering, and forming of the leads also help protect against component damage.

Dimensions — TO-263 (N-Package) — D² Pak Surface Mount



Dimension	Inches		Millimeters	
	Min	Max	Min	Max
A	0.360	0.370	9.14	9.40
B	0.380	0.420	9.65	10.67
C	0.178	0.188	4.52	4.78
D	0.025	0.035	0.64	0.89
E	0.045	0.060	1.14	1.52
F	0.060	0.075	1.52	1.91
G	0.095	0.105	2.41	2.67
H	0.092	0.102	2.34	2.59
J	0.018	0.024	0.46	0.61
K	0.090	0.110	2.29	2.79
S	0.590	0.625	14.99	15.88
V	0.035	0.045	0.89	1.14
U	0.002	0.010	0.05	0.25
W	0.040	0.070	1.016	1.78

Thyristors
35 Amp Alternistor (High Commutation) Triacs

Product Selector

Part Number		Gate Sensitivity Quadrants		$I_{T(RMS)}$	Type	Package
	600V	I – II – III	IV			
Q6035NAH5	X	50 mA		35A	Alternistor Triac	TO-263 D²-PAK

Note: xx = Voltage/10

Packing Options

Part Number	Marking	Weight	Packing Mode	Base Quantity
Q6035NAH5RP	Q6035NAH5	1.60 g	Embossed Carrier	500

xx = voltage/10

Part Numbering System

Q 60 35 N A H5

COMPONENT TYPE
Q : Triac or Alternistor Triac

VOLTAGE
60 : 600V

CURRENT
35 : 35A

PACKAGE TYPE
N: TO-263 (D²-PAK)

QUALIFICATION
A: AEC-Q101 Qualified

SENSITIVITY & TYPE
Alternistor Triac
H5 : 50mA (QI, II, III)

Part Marking System

TO-263 AB - (N Package)

Date Code Marking
Y:Year Code
M: Month Code
XXX: Lot Trace Code

TO-263 Embossed Carrier Reel Pack (RP) Specifications

Meets all EIA-481-2 Standards