

TVS Diode Arrays

TVS Rail Clamp Array in a Surface Mount Package

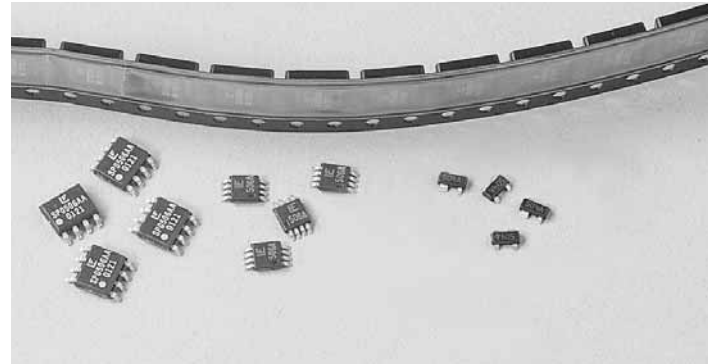
SP0502AAH, SP0506AAA, SP0506AAB

This family of rail clamp or “diode steering” arrays is designed for very low capacitance ESD protection and is offered in small surface mount packages. The multi-channel devices are used to help protect high speed sensitive digital or analog input circuits on data, signal, or control lines with unipolar voltage levels up to 5 VDC. The state-of-the-art structure is designed to suppress ESD and other transient over-voltage events to meet the International Electrotechnical Compatibility (IEC) transient immunity standards IEC 61000-4-2 for Electrostatic Discharge Requirements.

The monolithic silicon devices are comprised of specially designed low capacitance structures for transient voltage suppression (TVS). The size and shape of these structures have been tailored for transient protection. The low capacitance and clamp voltage are ideal for high speed signal line protection.

Ordering Information

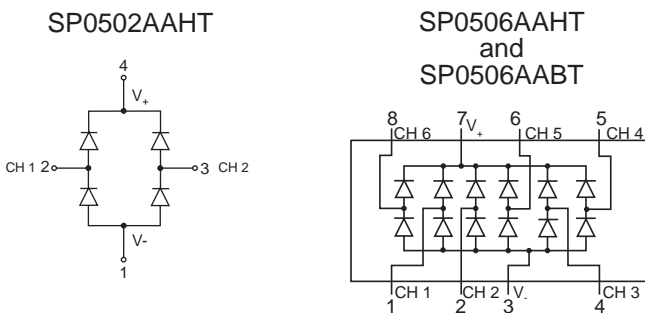
Part Number	CH	Package Type	Quantity Per Reel
SP0502AAHT	2	SOT143	3000
SP0506AAAT	6	MSOP8	4000
SP0506AABT	6	SOIC8	2500



Features

- A low capacitance 2, 6 and 18 channel array of rail clamp current steering diodes in small surface mount packages
- ESD Protection Capability (SP0502 and SP0506)
 - IEC 61000-4-2, Direct Discharge 8kV (Level 4)
 - MIL STD 3015.7 15kV
- ESD Protection Capability (SP0518)
 - IEC 61000-4-2, Direct Discharge 15kV (Level 4)
 - MIL STD 3015.7 15kV
- Input Protection for Applications Up to 5VDC
- Fast Response Time < 1ns
- Low Input Capacitance.3-7pF Typical
- Low Clamp Voltage $V_{rail} + 13V$ Max
- Operating Temperature Range. - 40°C to +85°C

Schematic



Applications

- Cell phone hand sets
- Personal Digital Assistants (PDA)
- Portable handheld equipment (Laptop, Palmtop computers)
- Computer port, keyboard (USB1.1)
- Digital cameras
- V6A port protection
- Digital still camera
- Digital video camera

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Electrical Specifications $T_A = 25^\circ\text{C}$ Unless Otherwise Specified

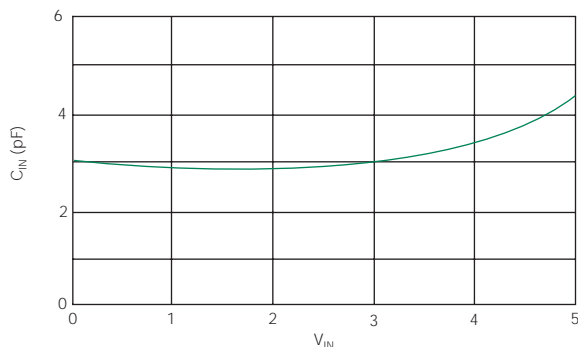
PARAMETER	TEST CONDITIONS	MIN	TYPICAL	MAX	UNITS
Operating Supply Voltage	$V_p - V_n$	-	-	6.0	V
Supply Current	$V_p - V_n = 5.5\text{V}$			10	μA
Channel Leakage Current			0.1	1.0	μA
Signal Clamp Voltage ⁽²⁾	15kV ESD HBM				
Positive				$V_p + 13$	V
Negative				$V_n - 13$	V
Diode Forward Voltage $I_f = 20\text{mA}$		0.65		0.95	V
Maximum Forward current ⁽¹⁾					
SP0502 and SP0506x				20	mA
Power Rating (SOT143)				275	μW
SOIC8				350	μW
MSOP8				200	μW
Maximum DC Input voltage		$V_n - 0.5$		$V_p + 0.5$	V
ESD Test Level (SP0502 and SP0506x) ⁽³⁾					
IEC-61000-4-2, Contact discharge		8			kV
MIL-STD-883 Method 3015 (HBM)		15			kV
Capacitance					
SP0502 and SP0506x	2.5VDC @ 1Mhz		3	5	pF
Turn on/off Time			<1		ns
Temperature Range					
Operating		- 40		+85	$^\circ\text{C}$
Storage		- 65		+150	$^\circ\text{C}$

SILICON PROTECTION CIRCUITS

- 1) One diode conducting at a time.
- 2) These parameters guaranteed by design and characterization.
- 3) From I/O pins to V_p or V_n only. V_p bypassed to V_n with a 0.22 μF ceramic capacitor.

Typical Capacitance

SP0502 and SP0506x



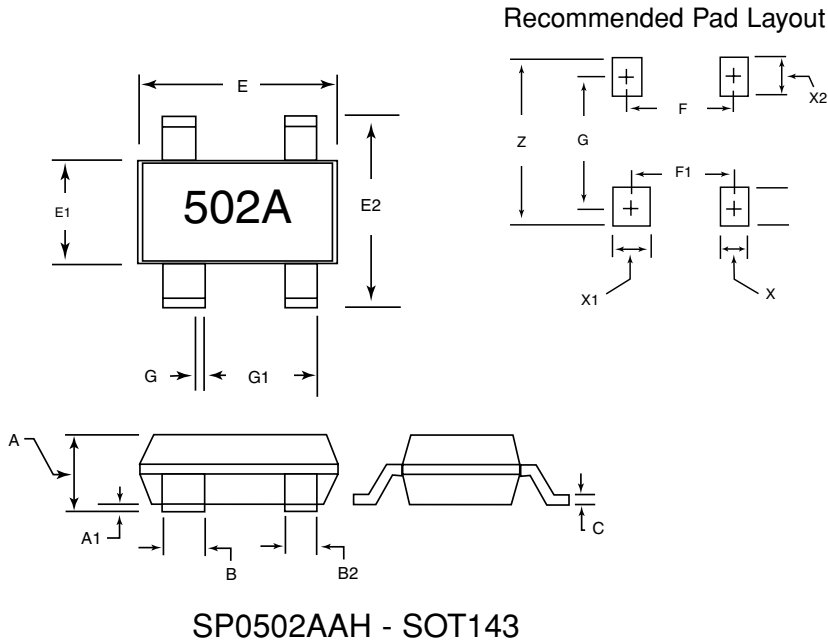
Typical Variation of C_{IN} with V_{IN}
 ($V_p=5\text{V}$, $V_n=0\text{V}$, 0.1 μF chip capacitor between V_p & V_n)

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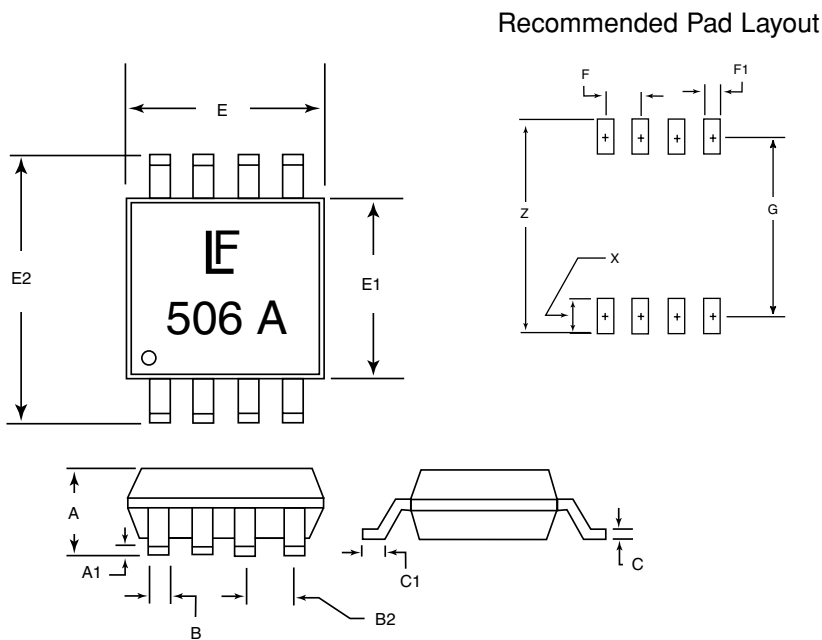
SP0502AAH, SP0506AAA, SP0506AAB

Outline Drawings



Package	SOT143			
	mm		inches	
	min	max	min	max
E	2.80	3.04	.110	.120
E1	1.20	1.40	.047	.055
E2	2.10	2.64	.083	.104
G	-	.020REF	-	1.920REF
G1	-	1.920REF	-	.076
A	0.890	1.120	.035	.044
A1	0.013	0.100	.0005	.0040
B	0.760	0.940	.030	.037
B2	0.370	0.510	.015	.020
C	0.0850	0.180	.0033	.0071
Z	3.40	3.60	.134	.140
G	-	2.2REF	-	.087REF
F	-	1.90	-	.075
F1	-	1.70	-	.067
X	0.80	1.00	.032	.040
X1	1.00	1.20	.040	.048
X2	-	1.40	-	.055

Outline Drawings



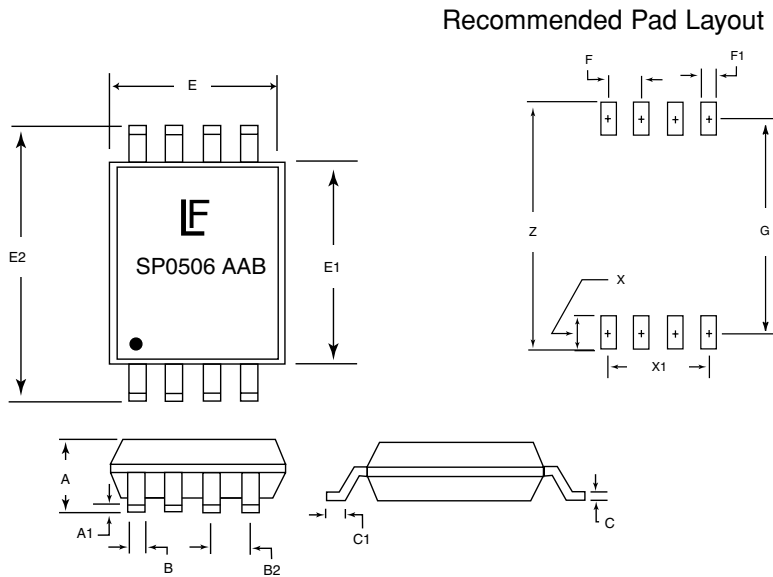
Package	MSOP 8			
	mm		inches	
	min	max	min	max
E	2.90	3.10	.114	.122
E1	2.90	3.10	.114	.122
E2	4.78	4.98	.188	.196
A	0.87	1.17	.034	.046
A1	0.05	0.25	.002	.010
B	-	0.30	-	.012TYP
B2	-	0.65	-	.25TYP
C	-	0.18	-	.007TYP
C1	0.52	0.54	.017	.025
F	-	0.65	-	.0256
F1	-	0.38	-	.015
Z	-	5.28	-	.208
X	-	1.04	-	.041
G	-	4.24	-	.167

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Outline Drawings



SP0506AAB - SOIC 8

Recommended Pad Layout

Package	SOIC 8			
	mm		inches	
	min	max	min	max
E	4.80	5.00	.189	.197
E1	3.80	4.19	.150	.165
E2	5.80	6.20	.228	.244
A	1.35	1.75	.053	.069
A1	0.10	0.25	.004	.010
B	0.33	0.51	.013	.020
B2	-	1.27	-	.050
C	0.19	0.25	.007	.010
C1	0.40	1.27	.016	.050
F	-	1.27	-	.05
F1	0.60	0.80	.02	.03
Z	7.20	7.40	-	.29
X	-	2.40	-	.09
X1	-	3.81REF	-	.15REF
G	-	5.00REF	-	.19REF

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SILICON PROTECTION CIRCUITS