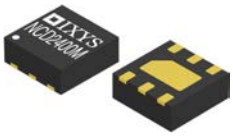
IXYS
INTEGRATED CIRCUITS DIVISION



NCD2400M

Wide Capacitance Range, Non-volatile Digital Programmable Capacitor

Features

- DC to 150MHz frequency range
- 512-state digital programmable capacitor
- Series or shunt configuration
  C_{shunt} = 12.5pF to 194pF (15.5:1 tuning ratio) in discrete 355fF steps
  C_{series} = 1.7pF to 194pF in discrete 376fF steps
- 2-wire (I^2C Fast-mode compatible) serial interface
- EEPROM non-volatile memory
- Wide power supply range (2.5V to 5.5V)
- Operation ambient temperature to 105ºC
- 2 x 2 x 0.65 mm 6-pin DFN package

Applications

- OCXOs
- Oscillators
- Tunable RF stages
- Filter tuning
- Capacitive sensor trimming
- Measurement equipment

Description

The NCD2400M is a dedicated electronic calibrator for oscillators, with reliable performance at 105ºC as required by OCXO applications.

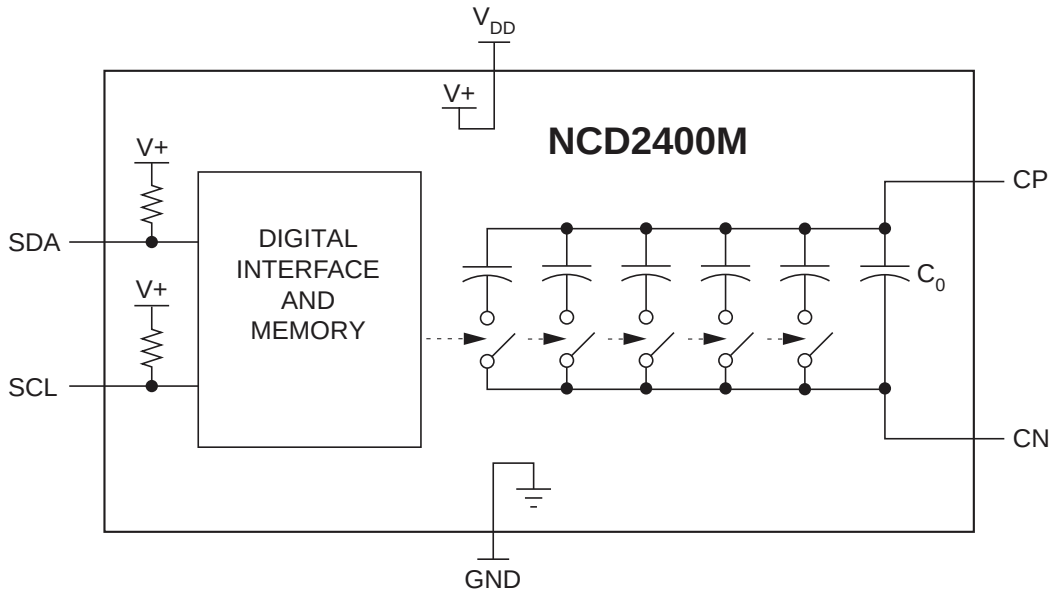
This product can be used in series or shunt configuration to support a wide variety of tuning circuit topologies.

Digitally controlled capacitance trimming information is communicated via a 2-wire, I^2C Fast-mode compatible interface. The preferred power-up default capacitance value can be stored in the internal, re-programmable, non-volatile memory.

Ordering Information

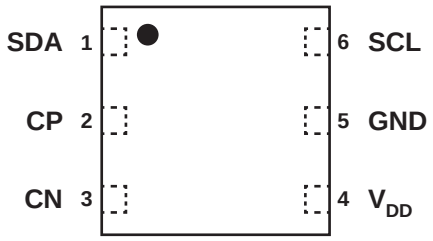
Part #	Description
NCD2400MTR	Standard product, Chip ID = 0x60, DFN-6 in Tape & Reel (3000/Reel)
NCD2400M1TR	Special order, Contact Factory for details, Chip ID = 0x61, DFN-6 in Tape & Reel (3000/Reel)

Figure 1. NCD2400M Block Diagram



1. Specifications

1.1 Package Pinout



1.2 Pin Descriptions

Pin	Name	Description
1	SDA	Serial data I/O
2	CP	Positive capacitance node
3	CN	Negative capacitance node
4	V_{DD}	Power supply
5	GND	Ground
6	SCL	Serial clock input

1.3 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
Supply voltage	-0.3	+ 6	V
SDA, SCL voltage	-0.3	V_{DD} + 0.3	V
CP voltage	-0.5	V_{DD} + 0.5	V
CN voltage			
V_{DD} < 3.3V	-0.5	V_{DD} + 0.5	V
V_{DD} ≥ 3.3V		3.8	
Operating temperature, T_A	-40	+105	°C
Storage temperature, T_{STG}	-55	+125	°C

Absolute maximum voltages are with respect to GND.

Absolute maximum electrical ratings are over the operating temperature range.

Absolute Maximum Ratings are stress ratings. Stresses in excess of these ratings can cause permanent damage to the device. Functional operation of the device at conditions beyond those indicated in the operational sections of this data sheet is not implied.

1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply voltage	V_{DD}	2.5	3.3	5.5	V
Capacitor voltage, CP or CN to GND [1, 2]					
V_{DD} < 3.3V	V_{CP}, V_{CN}	-0.3	-	V_{DD} + 0.3	V_{PK}
V_{DD} ≥ 3.3V				3.6	
Non-Volatile Write Programming time [3]	t_{PNV}	-	5	-	ms
Operating temperature	T_A	-40	-	+105	°C

[1] $V_{PK}=V_{DC}+V_{AC}$ is the voltage applied to capacitor pins CP and CN. It should never exceed 3.6V in operation, and should never be less than -0.3V. Sufficient DC bias must be applied to the capacitor pins to prevent the AC signal from violating this specification. Pins CP and CN are not self biased.

[2] These maximum values not to exceed the supply voltage; e.g. the maximum voltage drop between CN and GND is 2.8V when V_{DD}=2.5V.

[3] There are three erase commands and three non-volatile write commands to program the Non-Volatile Register. This time is for each of the three non-volatile write commands, not the sum of all three commands. The timing requirement also applies to each of the three erase commands, not the sum of all three.

1.5 ESD Rating

Parameter	Symbol	Conditions	Rating	Unit
Human body model	HBM	EIA/JESD22-A114-D	±2000	V
Charge device model	CDM	JS002-2014	±500	

1.6 General Conditions for Electrical Characteristics

Typical values are the result of engineering evaluations and are characteristic of the device at 25°C with V_{DD}=3.3V and pins CP and CN biased to 1.65V_{DC}. They are provided for informational purposes only and are not guaranteed by production testing.

Unless otherwise specified, specifications cover the operating temperature range T_A=-40ºC to +105ºC, and the supply voltage range V_{DD}= 2.5V to 5.5V.

1.7 Capacitor Electrical Characteristics

Unless otherwise noted, characteristics are at the nominal operating temperature of 25 ±5°C with the CP and CN terminals biased at one-half of the supply voltage.

Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Operating frequency range	-	-	-	-	150	MHz
Capacitance, Series Configuration	f=10MHz					pF
Minimum	Code=0	C_0	1.6	1.7	1.9	
Maximum	Code=511	C_{511}	177.3	194	209.2	
	f=50MHz					
Minimum	Code=0	C_0	1.6	1.7	1.9	
Maximum	Code=511	C_{511}	181.4	202.2	221.3	
Capacitance, Shunt Configuration[1]	f=10MHz					
Minimum	Code=0	C_0	11.5	12.5	13.5	
Maximum	Code=511	C_{511}	178.4	193.9	209.4	
	f=50MHz					
Minimum	Code=0	C_0	11.5	12.5	13.9	
Maximum	Code=511	C_{511}	188.8	203.0	229	
Tuning ratio, Shunt Configuration	C_{max} / C_{min}, f=10MHz	-	-	15.512:1	-	-
Step size, Series Configuration	Constant step size at f=10MHz	C_{step}	-	376.32	-	fF
Quality Factor	f=10MHz					-
	Code=0	QC_0	-	>150	-	
	Code=511	QC_{511}	35	95	-	
	f=50MHz					
	Code=0	QC_0	-	43	-	
	Code=511	QC_{511}	6.6	18.5	-	
Capacitance variation with temperature	-40°C ≤ T_A ≤ +105°C, f=10MHz	dC/dT	-	250	680	ppm/°C

[1] Shunt configuration: CP to Grounded CN

1.8 Digital Interface: Electrical Characteristics of SDA and SCL

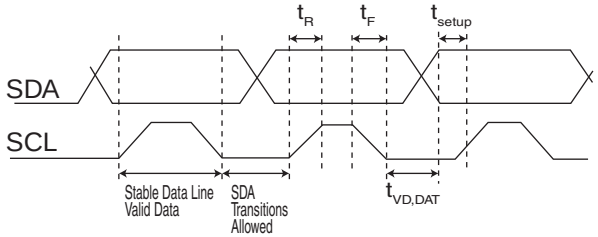
Parameter	Test Conditions	Symbol	Minimum	Typical	Maximum	Unit
Input voltage						
Logic 1 threshold	-	V_{IH}	$0.75V_{DD}$	-	-	V
Logic 0 threshold	-	V_{IL}	-	-	$0.25V_{DD}$	
Hysteresis	$V_{IH} - V_{IL}$	V_{HYS}	0.1	-	-	
SDA Output voltage [1]						
Logic 1	10kΩ pull-up resistor	V_{OH}	$0.95V_{DD}$	-	-	V
Logic 0	I_{OL} = 6mA	V_{OL}	-	-	0.4	
Pull-up resistors, Internal	T_A=25°C	R_{PU}	111	135	154	kΩ
	-40°C ≤ T_A ≤ +105°C		88	135	186	
Load capacitance	-	C_{LOAD}			400	pF

[1] SDA is an open drain pad. It is recommended to use a pull-up resistor with a value such that the current into pin SDA does not exceed 6mA, independent of the internal pull-up resistors.

1.9 Digital Interface: AC Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Serial clock (SCL)					
Frequency	f_{SCL}	-	-	400	kHz
Duty cycle	D_{SCL}	40	-	60	%
Rise / fall times	t_R / t_F	-	-	100	ns
Serial data (SDA)					
Setup time	t_{setup}	300	-	-	ns
Rise / fall times	t_R / t_F	-	-	100	
Data valid time[1]	$t_{VD,DAT}$	-	-	180	ns
Non-Volatile Write Programming time [2, 3]	t_{PNV}	4		8	ms

[1] R_P = 1kΩ, C_{LOAD} = 100pF
[2] Programming time begins with the falling edge of CLK just after the CONFIG 0 ACK and ends with the rising Stop bit edge on SDA.
[3] This time is for each non-volatile write commands, not the sum of all three commands.



Note: SDA output transitions occur only when SCL is low, as shown in the following timing diagram.

1.10 Power Supply

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Supply voltage	V_{DD}	2.5	3.3	5.5	V
Supply current	I_{DD}	-	50	90	µA

2. Performance Data

Note: The performance data shown in the graphs below is the measured performance at ambient temperature.

The typical shunt and series capacitance, in pF, varies as indicated in the following equations:

$$C_{OUT} = C_0 + C_{var}$$

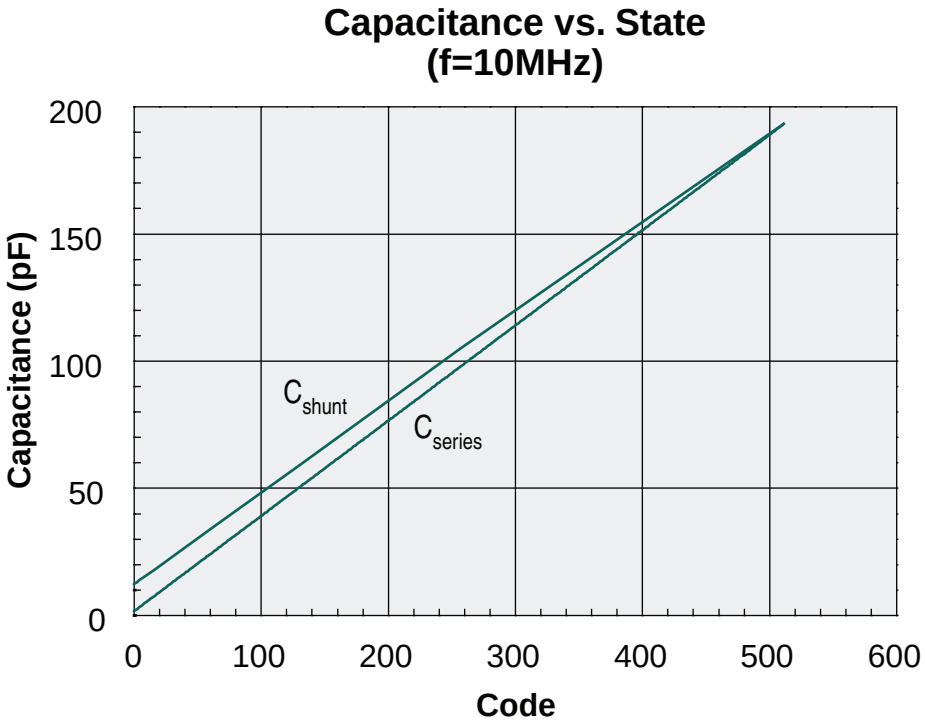
$$C_{shunt} = 12.5 + 0.355 \bullet \text{Code}$$

$$C_{series} = 1.7 + 0.376 \bullet \text{Code}$$

Where Code = 0 to 511.

Other performance aspects of the programmable capacitor are illustrated in the graphs below.

Figure 1: Shunt and Series Capacitance vs. Code



In shunt configuration, the parasitic capacitance from pin CP to GND adds up to the total equivalent capacitance of the device. The expected values are the ones defined by the above equation. In series configuration, though, this parasitic capacitor is not part of the equivalent impedance of the device, therefore the overall capacitance seen between CP and CN is smaller.

Figure 2: Series Capacitance vs. Frequency for Code 64 to Code 511

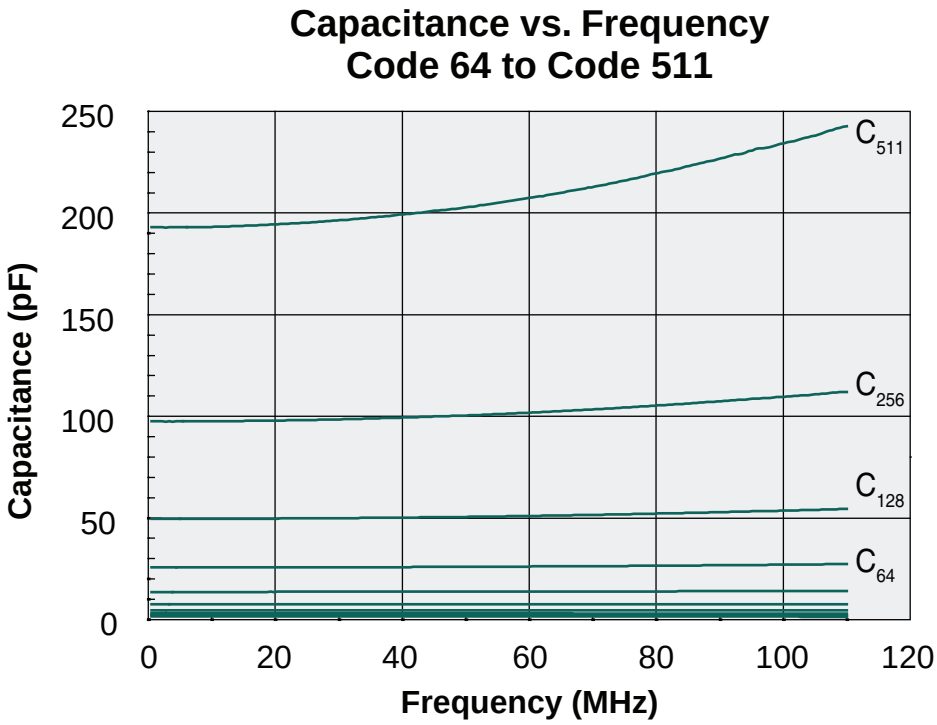


Figure 3: Series Capacitance vs. Frequency for Code 0 to Code 64

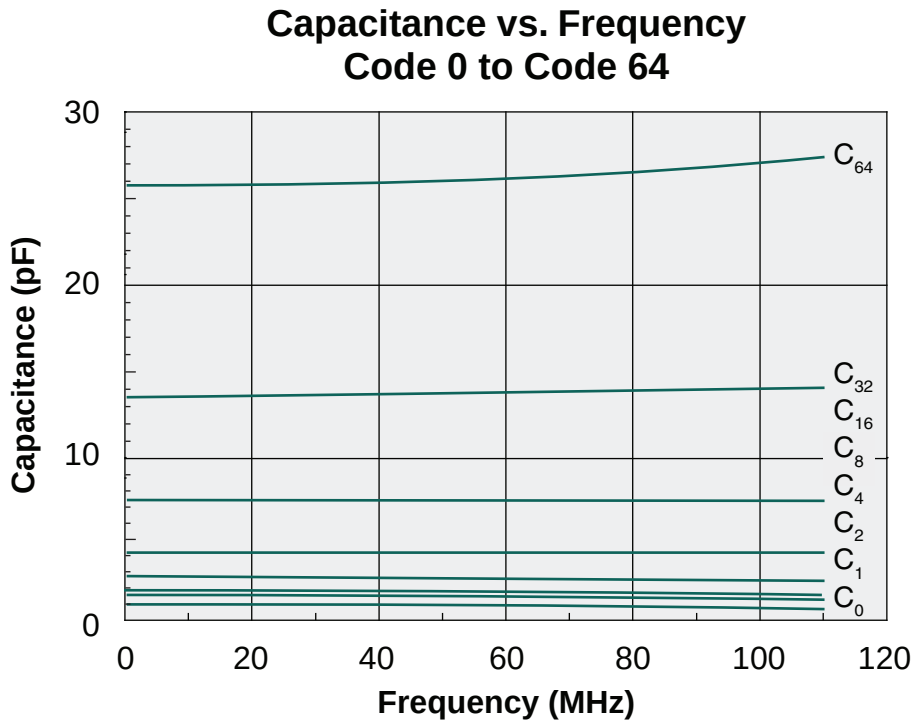


Figure 4: Quality Factor vs. Frequency and Code

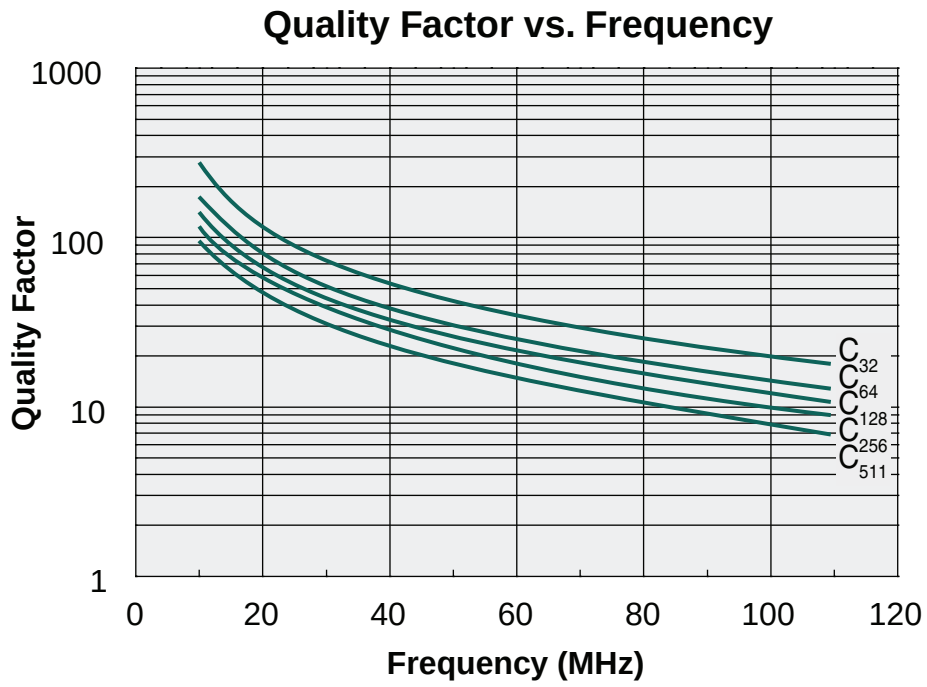
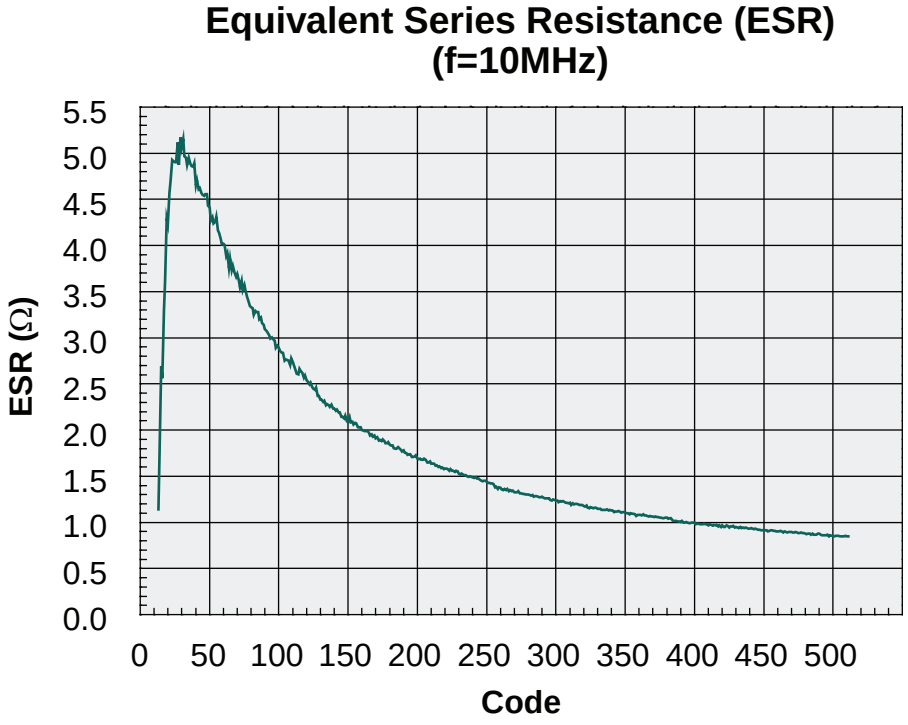
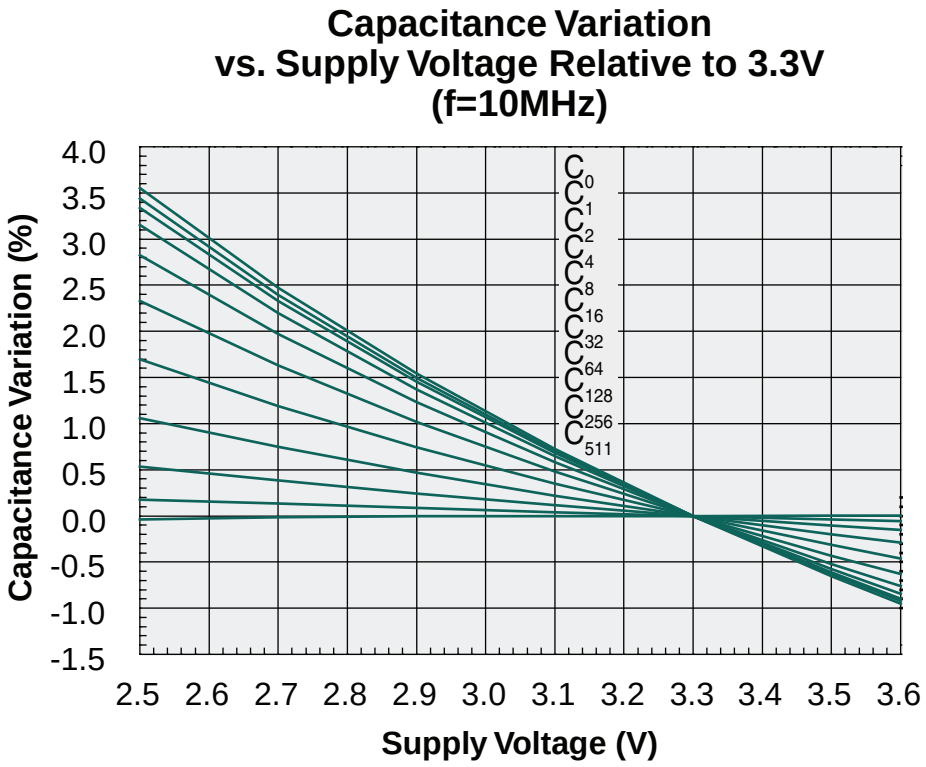


Figure 5: ESR vs. Code for Nominal Operation Conditions



The figure below shows how the capacitance varies with the supply voltage while CN is biased at one-half of the supply voltage level. Here, the value obtained for 3.3V is used as a reference and the deviation is given in percentage. Please note that for V_{DD} > 3.6V no further variations are expected.

Figure 6: Variation of the Capacitance at 10MHz with Supply Voltage, Relative to the Value at 3.3V



DC voltage biasing of the CN terminal has a small though visible influence on the performance of the Digital Programmable Capacitor. The table below presents the variation of the series capacitance and ESR at 10MHz when pin CN is biased at 0V, 1.65V and 3.3V, with V_{DD}=3.3V. DC bias applied to pin CP has no affect on the capacitance or ESR values.

	Capacitance (pF)			ESR (Ω)		
Code / V_{bias} (V)	0	1.65	3.3	0	1.65	3.3
0	1.7	1.7	1.9	0.509	0.442	0.695
1	2.1	2.1	2.3	0.739	0.720	1.006
2	2.5	2.5	2.7	0.949	0.973	1.29
4	3.2	3.2	3.5	1.271	1.366	1.742
8	4.7	4.7	5.1	1.754	1.952	2.431
16	7.6	7.7	8.2	2.256	2.564	3.188
32	13.7	13.7	14.3	4.342	4.968	6.31
64	25.6	25.6	26.4	3.259	3.755	4.882
128	49.6	49.6	50.3	2.063	2.372	3.14
256	97.4	97.5	98.1	1.204	1.377	1.827
511	193.2	194	193.2	0.75	0.846	1.106

The equivalent shunt capacitance changes for small variations of the supply voltage around the nominal value. The following table shows the deviation of the equivalent shunt capacitance for a 200mV change of the supply voltage from 3.3V.

Relative deviation of the capacitance with respect to the supply voltage around nominal value of 3.3V.											
Parameter	Code 0	Code 1	Code 2	Code 4	Code 8	Code 16	Code 32	Code 64	Code 128	Code 256	Code 511
pF/V	-0.22	-0.22	-0.22	-0.22	-0.22	-0.21	-0.21	-0.19	-0.17	-0.11	-0.01

For a deviation of +200mV in supply voltage, the capacitance for Code 0 will be modified by -0.044pF. Using the previously-stated equation for calculating the nominal values of C_{shunt} it can be expected the nominal value of C_{shunt} will shift from 12.5pF to 12.456pF. Similarly, for a supply voltage change of -200mV, the nominal value of C_{shunt} will be 12.5pF - (-0.044pF) = 12.544pF.

3. Functional Description

3.1 Introduction

The NCD2400M provides a digitally controlled variable output capacitance between pins CP and CN. This capacitance can be used as a series capacitor (between CP and CN) or a shunt capacitor (connecting CN to GND). Do not connect CP to GND.

The output capacitance is set by either the content of the Volatile Register or by the content stored in the re-programmable Non-Volatile Memory.

Upon power-up, the default capacitance value between CP and CN is determined by the digital value stored in the non-volatile memory. The capacitance can, however, be controlled directly with the content of the Volatile Register.

The output capacitance presented by the NCD2400M between pins CP and CN is defined by:

$C_{OUT} = C_0 + C_{var}$

Where:

- C_0 is the base output capacitance (Code 0) and
- C_{var} is the variable tuning capacitance, whose value is set by the 9-bit CDAC control word

The NCD2400M has two operating modes related to the way the programmable capacitor is controlled: Volatile and Non-Volatile.

- Volatile Mode: the Control Data value in the Volatile Register determines the output capacitance.
- Non-Volatile Mode (Default mode): the Control Data value stored in the Non-Volatile Memory determines the output capacitance.

In Non-Volatile Mode, the default mode, the Control Data value is determined by the content programmed into the non-volatile memory. This mode is useful in situations where the required output capacitance is unlikely to change and the control data must be retained during periods of no power.

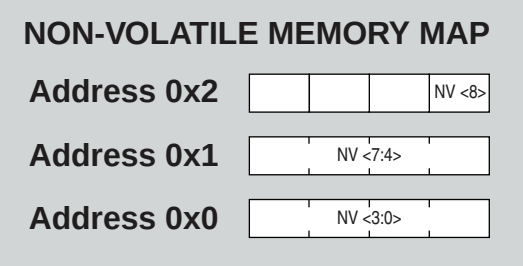
3.2 Capacitive Digital to Analog Converter (CDAC)

The nine bits in the Capacitive Digital to Analog Converter constitute the control bits of the variable capacitor. Shown in the table below are the expected typical capacitance values of several codes for the series configuration.

Decimal	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	C_{OUT} (pF)
0	0	0	0	0	0	0	0	0	0	1.70
1	0	0	0	0	0	0	0	0	1	2.08
2	0	0	0	0	0	0	0	1	0	2.45
3	0	0	0	0	0	0	0	1	1	2.83
4	0	0	0	0	0	0	1	0	0	3.20
5	0	0	0	0	0	0	1	0	1	3.58
6	0	0	0	0	0	0	1	1	0	3.96
7	0	0	0	0	0	0	1	1	1	4.33
125	0	0	1	1	1	1	1	0	1	48.70
126	0	0	1	1	1	1	1	1	0	49.08
127	0	0	1	1	1	1	1	1	1	49.45
128	0	1	0	0	0	0	0	0	0	49.83
250	0	1	1	1	1	1	0	1	0	95.70
251	0	1	1	1	1	1	0	1	1	96.08
252	0	1	1	1	1	1	1	0	0	96.45
253	0	1	1	1	1	1	1	0	1	96.83
254	0	1	1	1	1	1	1	1	0	97.20
255	0	1	1	1	1	1	1	1	1	97.58
256	1	0	0	0	0	0	0	0	0	97.96
499	1	1	1	1	1	0	0	1	1	189.32
500	1	1	1	1	1	0	1	0	0	189.70
501	1	1	1	1	1	0	1	0	1	190.08
502	1	1	1	1	1	0	1	1	0	190.45
503	1	1	1	1	1	0	1	1	1	190.83
504	1	1	1	1	1	1	0	0	0	191.20
505	1	1	1	1	1	1	0	0	1	191.58
506	1	1	1	1	1	1	0	1	0	191.96
507	1	1	1	1	1	1	0	1	1	192.33
508	1	1	1	1	1	1	1	0	0	192.71
509	1	1	1	1	1	1	1	0	1	193.08
510	1	1	1	1	1	1	1	1	0	193.46
511	1	1	1	1	1	1	1	1	1	193.84

3.3 Non-Volatile Memory Configuration

The 9-bit CDAC code stored in non-volatile memory is organized in three addressable nibbles as shown below:



3.4 Device Address

NCD2400M has two available 7-bit device addresses (Chip ID) hard-coded during manufacturing. These are shown in the table below.

Address Selection			
Model	Address (HEX)	Address (BIN)	Address (DEC)
NCD2400M	0x60	1100000	96
NCD2400M1	0x61	1100001	97

This simple way of addressing allows for easy configuration in systems that employ up to two NCD2400M slaves.

3.5 Operating Modes

The NCD2400M functions in one of two modes, Volatile and Non-Volatile.

The output capacitance between CP and CN can be controlled by the value loaded into the volatile register (Volatile Mode), or by reading the value stored in the non-volatile memory (Non-Volatile Mode).

3.5.1 Volatile Mode

Volatile Mode provides the means to alter the output capacitance at any time. Because Volatile Mode is functional over the entire operational range of the NCD2400M, the capacitance presented between CP and CN can be modified under all allowed operating conditions. Modifying the capacitance in Volatile Mode is easily accomplished by writing the 9-bit CDAC control code into the Volatile Register (VR), using the I^2C interface.

Anytime data is written into the Volatile Register, Volatile Mode is automatically enabled and remains active until a loss of power or the “Set Non-Volatile Mode” command is received. The contents of the volatile register will be lost whenever power to the device is removed.

3.5.2 Non-Volatile Mode

Non-Volatile Mode is the default mode of operation and uses the value stored in the Non-Volatile memory (NV) to configure the capacitor.

By default, upon power up, the NCD2400M operates in the Non-Volatile Mode. This is advantageous for applications where reprogramming the capacitance value is not convenient or for applications where the end product may be subjected to an unreliable power environment.

Non-Volatile Mode is entered into automatically at power up, or after receiving the “Set Non-Volatile Mode” command.

3.6 I^2C Serial Interface

The NCD2400M digitally controlled variable capacitor can be accessed by an I^2C serial interface. The NCD2400M can only act as a Bus Slave. The Bus Master initiates the start of a serial transaction by driving SDA (Serial Data) low while SCL (Serial Clock) is high. This is the Start bit. Data bit transitions on SDA are permitted only when SCL is low and are clocked in by the receiver on the rising edge of SCL. A logic low (0) Acknowledge (ACK) bit is output onto the SDA bus by the NCD2400M following each received byte.

Depending on the value of the Read/$\overline{\text{Write}}$ (R/$\overline{\text{W}}$) bit following the 7-bit device address (Chip ID), a read or write command will be executed.

Four operations are available through the serial interface:

- Write Volatile Register
- Write Non-Volatile Memory
- Read
- Set Non-Volatile Mode

3.6.1 Write Commands

With a valid device address and the R/$\overline{W}$ bit set to 0, the NCD2400M will execute a write operation. The 8-bit address byte follows the Start bit and consists of two parts, first the device 7-bit Chip ID then the R/$\overline{W}$ bit located in the byte's least significant bit (LSB) position. For a given device Chip ID, the address byte is the same for all write commands.

Following the device address byte, for all write commands, the Master will send two CONFIG data bytes containing information to control the device and when the output capacitor value is to be modified, CDAC codes. As with the address byte, both CONFIG 1 and CONFIG 0 are 8-bit bytes.

The three realizable operations by means of the write command are:

- Write Volatile Register
- Write Non-Volatile Memory
- Set Non-Volatile Mode

3.6.2 Write Volatile Register Operation

The Write Volatile Register Operation takes data from the Configuration Bytes and stores it in the Volatile Register. Additionally, anytime the Write Volatile Register Operation is executed, the NCD2400M will be placed into the Volatile Mode. In order to return to the Non-Volatile Mode the device will need to be power cycled or sent a "Set Non-Volatile Mode" command

A Write Volatile Register command issued by the bus Master consists of the device address byte followed by two CONFIG byte sequences: CONFIG 1 then CONFIG 0.

CONFIG 1 consists of the NV/$\overline{V}$ control bit, six Don't Care bits, and the MSB of the CDAC code to be written into the Volatile Register. Setting NV/$\overline{V}$ = 1 specifies a Non-Volatile Memory write operation and when NV/$\overline{V}$ = 0, a Volatile Register write operation will be executed.

The most significant bit (MSB) of CONFIG 1, CONFIG 1 <7> is the NV/$\overline{V}$ control bit. For a Volatile Register write the next six bits, CONFIG 1 <6:1>, are Don't Care bits while the last bit, CONFIG 1 <0> is the MSB of the CDAC code being written.

Located between the NV/$\overline{V}$ and CDAC MSB bits are the six Don't Care bits. Their value has no effect on the outcome of the Volatile Register write operation. Since a logic 0 on an I^2C bus is the dominant state, it is recommended these six bits be set to 0 in applications where the bus is shared with other devices or where the unit is located in a noisy environment.

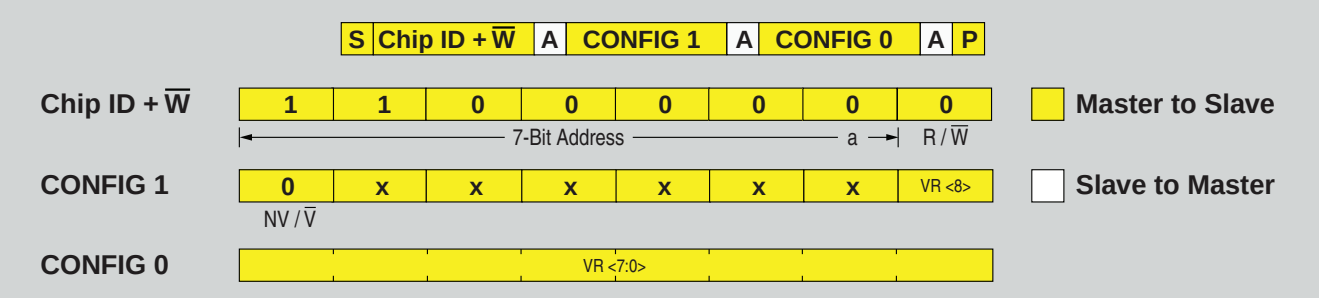
The nine bit CDAC data to be written into the volatile register is contained within the two Configuration Bytes as such:

- CDAC<8> bit is the last bit (LSB) of CONFIG 1
- CDAC<7:0> bits are the CONFIG 0 <7:0> bits.

The CDAC bits map directly to the Volatile Register such that CDAC<8> = VR<8>, CDAC<7> = VR<7>, and so on.

The data transfer format for writing to the Volatile Register (NV/$\overline{V}$ = 0) is shown below for a device with Chip ID 0x60.

WRITE OPERATION: VOLATILE REGISTER



NOTE: In the diagram above, bit "a" in the address byte is the LSB of the Chip ID. Set this bit to 1 when addressing the NCD2400M1 device as its Chip ID address is 0x61.

3.6.3 Write Non-Volatile Memory Operation

A Write Non-Volatile Operation takes data from the Configuration Bytes and stores it in the Non-Volatile Memory. Unlike the Write Volatile Register Operation, the Write Non-Volatile Operation does not change the operating mode of the device. Therefore, a Write Non-Volatile Memory Operation may be performed while the device is operating in either the Volatile or the Non-Volatile mode.

Although the CDAC code stored in the non-volatile memory is nine bits, the same as the Volatile Register, programming the non-volatile memory requires a write command for each addressable memory nibble. Furthermore, each nibble must be erased before being written.

The data structure of the two CONFIG bytes is the same for all three memory nibbles. CONFIG 1 contains the NV/$\overline{V}$ control bit, the two bit memory nibble address, the “Set Non-Volatile Mode” control bit, and four Don’t Care bits. CONFIG 0 contains the CDAC data bits preceded by sufficient Don’t Care bits to fill the byte. For an erase operation, CONFIG 0 is always four Don’t Care bits followed by 0x0.

In CONFIG 1 <7> (MSB), setting NV/$\overline{V}$ = 1 selects writing the incoming data to the Non-Volatile Memory. Following the NV/$\overline{V}$ bit in CONFIG 1 <6:5> are the two non-volatile memory address bits, then the Set Non-Volatile Mode control bit and four Don’t Care bits to complete the byte. The two bit non-volatile memory address MSB is placed in CONFIG 1 <6> with the LSB following in CONFIG 1 <5>. In CONFIG 1 <4> is the Set Non-Volatile Mode control bit which must be set to a logic 0 for a non-volatile write command. The last four bits, CONFIG<3:0> are Don’t Care bits.

The 9-bit CDAC data to be written into the non-volatile memory is embedded within the CONFIG 0 byte across three write commands.

Shown in the table below is the data structure of the three CONFIG 1 and CONFIG 0 bytes required to program a new 9-bit CDAC code into the non-volatile memory or to erase the memory. Lower case “x” in CONFIG 1 and CONFIG 0 indicates a Don’t Care bit value.

MEMORY ADDRESS	CONFIG 1	CDAC DATA CONFIG 0	ERASE CONFIG 0
0x2	1100 xxxx	xxxxxxx CDAC<8>	xxxx 0000
0x1	1010 xxxx	xxxx CDAC<7:4>	xxxx 0000
0x0	1000 xxxx	xxxx CDAC<3:0>	xxxx 0000

The CDAC bits map directly to the Non-Volatile Memory such that CDAC<8> = NV<8>, CDAC<7> = NV<7>, and so on.

The three addressable Non-Volatile Memory nibbles may be treated as independent entities. This means they may be written in any order and do not all have to be written to update the value stored in memory. If desired, just one or two can be updated, leaving the non-updated nibbles at their current value.

The duration of each non-volatile write operation must satisfy the **Non-Volatile Write Programming time** specified in **Section 1.4 "Recommended Operating Conditions” on page 3**. The programming time is defined as the period from the falling CLK edge just after the CONFIG 0 ACK bit output by the NCD2400M until the rising Stop bit edge on SDA output by the bus master.

In the example below, WAIT bytes are sent on the SDA data bus for the programming time duration. Using WAIT bytes with value 0x00 prevents other devices on the bus or noise from interfering with the NCD2400M internal programming process. Alternatively, in a well controlled environment the WAIT bytes need not be applied. Holding CLK, the serial clock, low (Logic 0) to lock up the I^2C bus to satisfy the programming time duration is acceptable. A Stop bit is required to terminate the programming time duration, ending the NCD2400M internal programming procedure.

Failure to comply with the programming time requirements may result in failure of the non-volatile memory to retain its stored information or damage to the device.

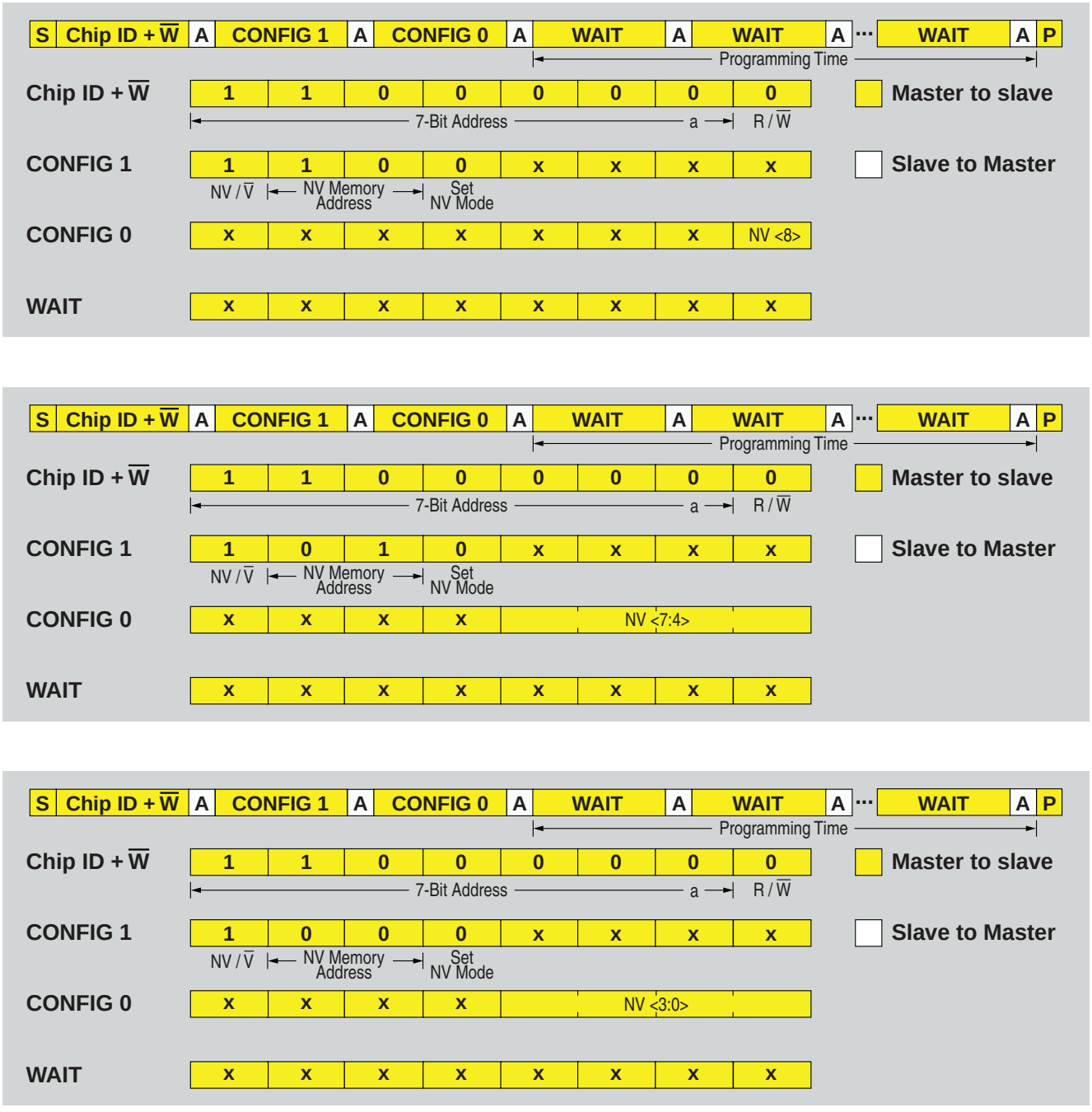
Following the Non-Volatile Write sequence, a Read command or a power up reset must be executed to update the contents of the CDAC non-volatile control register with the new memory value. If the NCD2400M is operating in the Volatile Mode during the Non-Volatile write operation, then a “Set Non-Volatile Mode” command must be executed **after** the Read command for the programmable capacitor value to reflect the new memory value.

Prior to writing new data into the non-volatile memory the existing data must be erased. The erase operation is a non-volatile write with CONFIG 0 = xxxx0000. A Read command is not required following an erase operation *unless* the change is to set the memory nibble(s) value to 0x0.

In the programming example below, the three memory nibbles are being written with address 0x2 first and 0x0 last.

The logical structure of a Write Non-Volatile Memory Operation is provided in the diagram below.

WRITE OPERATION: NON-VOLATILE MEMORY



The logic diagram above is for writing new CDAC data into memory, not an erase operation.

3.6.4 Read Operation

With a valid device address and the R/$\overline{W}$ bit set to 1, the device will execute a Read Operation. Following the device address byte from the Master, the NCD2400M slave will output 4 bytes on the SDA bus: BYTE 3 will be output first; followed by BYTE 2; then BYTE 1; and last BYTE 0.

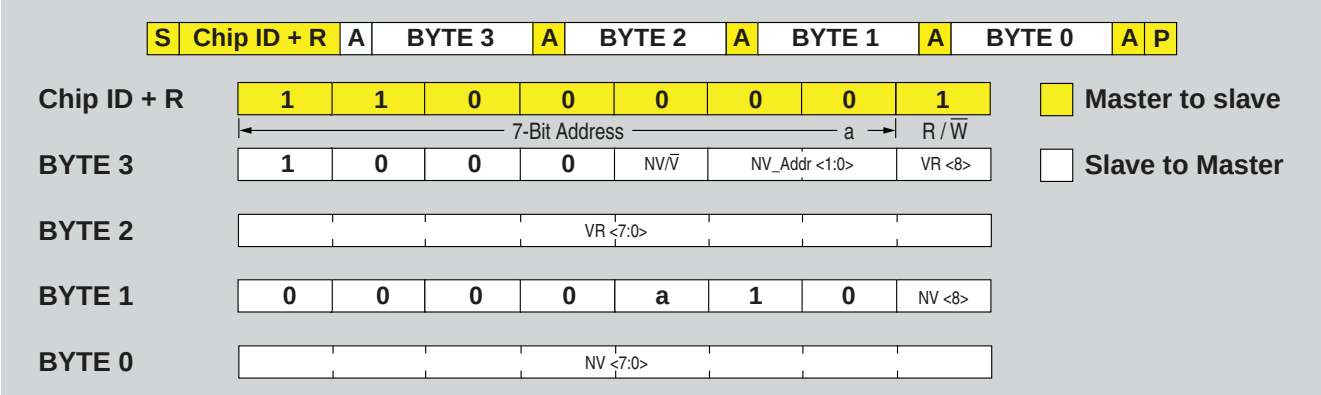
- BYTE 3: bits <7:4> = 0x8; bit <3> is nv/$\overline{v}$, the current Operating Mode (1 = Non-Volatile), (0 = Volatile); bits<2:1> Address of last written Non-Volatile nibble; and bit <0> is vr<8>, the Volatile Register MSB
- BYTE 2: bits <7:0> are vr<7:0>, the Volatile Register bits <7:0>
- BYTE 1: bits <7:4> = 0x0; bit <3> is “a”, the I^2C Chip ID address LSB; bits <2:1> = 0x2; and bit <0> is nv<8>, the Non-Volatile memory MSB
- BYTE 0: bits <7:0> are nv<7:0>, the Non-Volatile memory bits <7:0>.

A read command instructs the NCD2400M to perform two tasks. Data in Non-Volatile Memory is passed to the CDAC non-volatile controller register which configures the programmable capacitor when operating in the Non-Volatile Mode. And second, the NCD2400M will output its stored contents onto the SDA bus as described above. The content output onto the bus of the Volatile Register and the Non-Volatile Memory is the last data written into these locations.

Reading the device after a power up reset and before a write to the Volatile Register will return a value of 0x000 for the contents of the Volatile Register. This is because the Volatile Register is cleared at power up.

When the device is returned to the Non-Volatile Mode by means of the “Set Non-Volatile Mode” command, a read operation will return the last value written into the Volatile Register. Data format of a read operation is illustrated in the diagram below

READ OPERATION.



3.6.5 Set Non-Volatile Mode Operation

A valid Device Address with the R/$\overline{W}$ bit set to 0, and CONFIG1 configured as shown below, the device will convert to the Non-Volatile Mode.

The NCD2400M Set Non-Volatile command changes the operating mode from Volatile to Non-Volatile. This is accomplished by using a non-volatile write command. The command data structure uses only the upper nibble of CONFIG 1 by setting CONFIG 1<7:4> to 0x9. The upper nibble consists of: CONFIG 1<7>, the NV/$\overline{V}$ control bit; CONFIG 1<6:5>, the non-volatile memory address; and CONFIG 1<4>, the Set Non-Volatile Mode control bit. The lower nibble bits, CONFIG 1<3:0>, are Don't Cares.

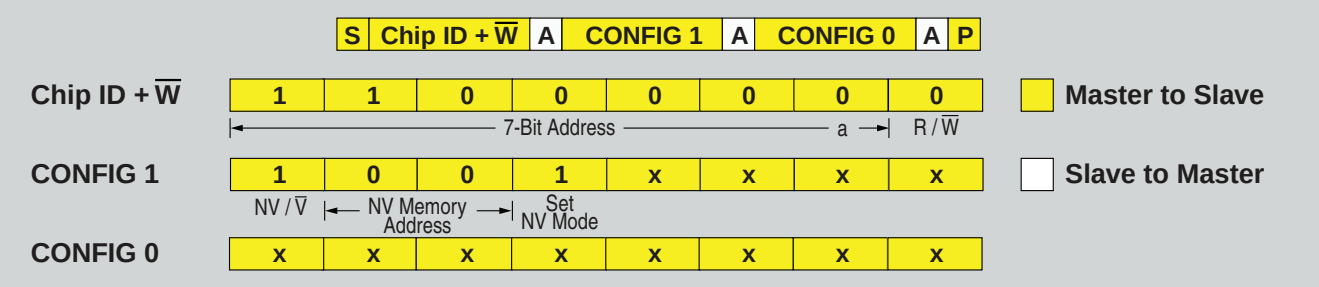
Additionally, all of CONFIG 0 bits of the Set Non-Volatile command are Don't Cares.

Once this operation is executed, the NCD2400M will be operating in the Non-Volatile Mode and the output capacitance value will reflect the value stored in the Non-Volatile CDAC. A Read command or power up reset is required to pass any updated value stored in the Non-Volatile Memory to the Non-Volatile CDAC.

This operation does not alter the contents of the Volatile Register. Therefore any Read command after the Set Non-Volatile Mode will reflect the last CDAC code written to the volatile register. A power up reset will clear the register contents.

The data format for the Set Non-Volatile Mode command is shown in the diagram below

SET NON-VOLATILE MODE OPERATION.



3.6.6 Electrical and Timing Considerations

The electrical and timing conditions that must be followed for reliable programming are provided in **Section 1.8 "Digital Interface: Electrical Characteristics of SDA and SCL"** and **Section 1.9 "Digital Interface: AC Characteristics" on page 5** and are repeated below for convenience.

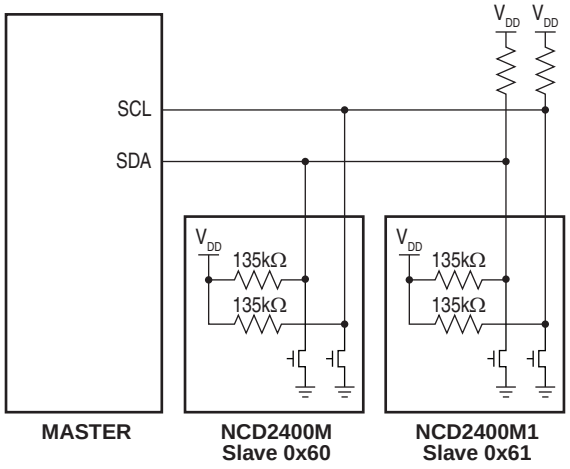
Internal pull up resistors at SDA and SCL with a nominal value of 135kΩ maintain an inert logic '1' state at these inputs to ensure stable and predictable behavior without the need for supplementary external components for lightly loaded busses. This is especially useful for customers who want to do one time programming and do not need to adjust the capacitance value during normal operation. For these applications the pins may be left unterminated.

Configuring or programming the NCD2400M must be done under the following conditions:

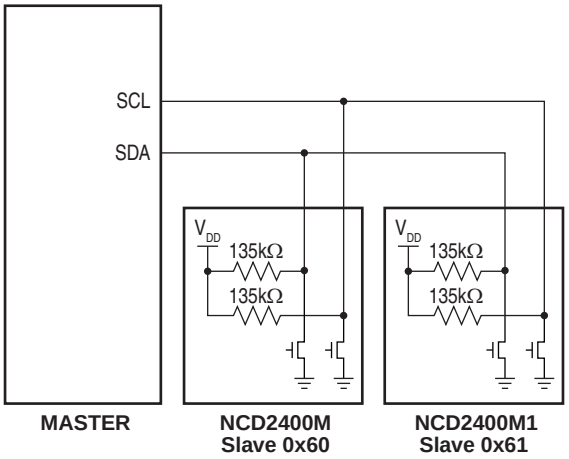
- Serial Clock: f_{SCL}= 400kHz max.
- Serial Clock: D_{SCL}= 50% ± 10%
- Non-Volatile programming, nominal duration t_{PNV} = 5ms.

3.6.7 Application Diagrams

The recommended application circuit for I^2C communication between the Master and two NCD2400M devices operating as slaves, is shown in the diagram below. It is recommended to use properly valued pull-up resistors on both the SDA and SCL nets to accommodate any additional devices attached to the bus and loading due to the PCB interconnection traces.



For applications where there are no other devices on the bus and the capacitance loading of the interconnection traces is low, it may be possible to avoid using external pull-up resistors by using only the internal pull-up resistors.



3.7 Capacitor Interface Electrical and Biasing Considerations

Proper biasing of the capacitor pins CP and CN is required to ensure analog performance of the NCD2400M. Because these pins are not self biased, it is necessary for the user to provide the required DC bias with sufficient headroom for the AC waveform thereby preventing signal distortion caused by clipping. Additionally the maximum signal level into these pins must not be exceeded. The voltage limitations for CP and CN are given in **Section 1.4 "Recommended Operating Conditions" on page 3**.

4. Capacitance Determination and Programming Procedure

Users who want to operate the NCD2400M in the Non-Volatile Mode upon power up will need to preprogram the appropriate CDAC code into memory. The two phases of this procedure are:

- Capacitance Code Determination
- Capacitance Code Programming

Trimming the NCD2400M capacitance to the optimal value is best accomplished in the Volatile Mode. CDAC code changes to the Volatile Register require fewer I^2C write operations and the capacitance value change is immediate, no need to perform a Read command to execute the code update.

Once the code for the desired capacitance value is known, it needs to be stored in the Non-Volatile memory by means of the Non-Volatile write command. Three separate write commands are required to program all three nibble of the Non-Volatile memory.

Before writing a new code into the Non-Volatile Memory it must be erased in order to delete any old content.

The recommended procedure for this is given below.

For a device with address 0x60, the sequence to write capacitance codes 0x125, 0x126, 0x127 and 0x128 to the Volatile Register and then programming 0x127 into the Non-Volatile Memory is as follows:

- All commands will be to device address 0x60.
- Write 0x125 into the Volatile Register.
- Write 0x126 into the Volatile Register.
- Write 0x127 into the Volatile Register.
- Write 0x128 into the Volatile Register.
- Write 0x127 into the Non-Volatile Memory using following sequence:
    - Erase memory nibble 0x0: Write 0x0 into non-volatile memory address 0x0
    - Write 0x7 into non-volatile memory address 0x0
    - Erase memory nibble 0x1: Write 0x0 into non-volatile memory address 0x1
    - Write 0x2 into non-volatile memory address 0x1
    - Erase memory nibble 0x2: Write 0x0 into non-volatile memory address 0x2
    - Write 0x1 into non-volatile memory address 0x2
- Read the memory content using the Read command.
- Set Non-Volatile mode. Note that the capacitance value won't change and will correspond to the content of the Volatile Register unless the mode is changed to Non-Volatile.

Different sequences than the one described above, such as erasing all memory nibbles before writing new values to them, are permitted.

5. Manufacturing Information

5.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits Division classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
NCD2400M - All Versions	MSL 1

5.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

5.3 Soldering Profile

Provided in the table below is the Classification Temperature (T_C) of this product and the maximum dwell time the body temperature of this device may be (T_C - 5)ºC or greater. The classification temperature sets the Maximum Body Temperature allowed for this device during lead-free reflow processes. For through-hole devices, and any other processes, the guidelines of J-STD-020 must be observed.

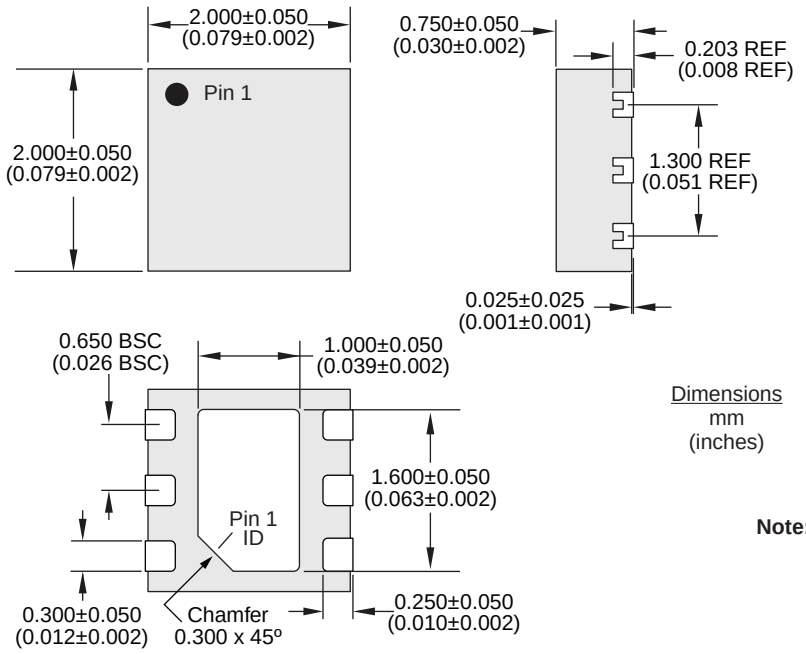
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
NCD2400M - All Versions	260°C	30 seconds	3

5.4 Board Wash

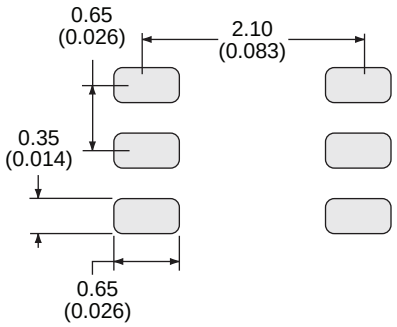
IXYS Integrated Circuits Division recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to flux or solvents that are Chlorine- or Fluorine-based.

5.5 Mechanical Dimensions

5.5.1 Package Dimensions



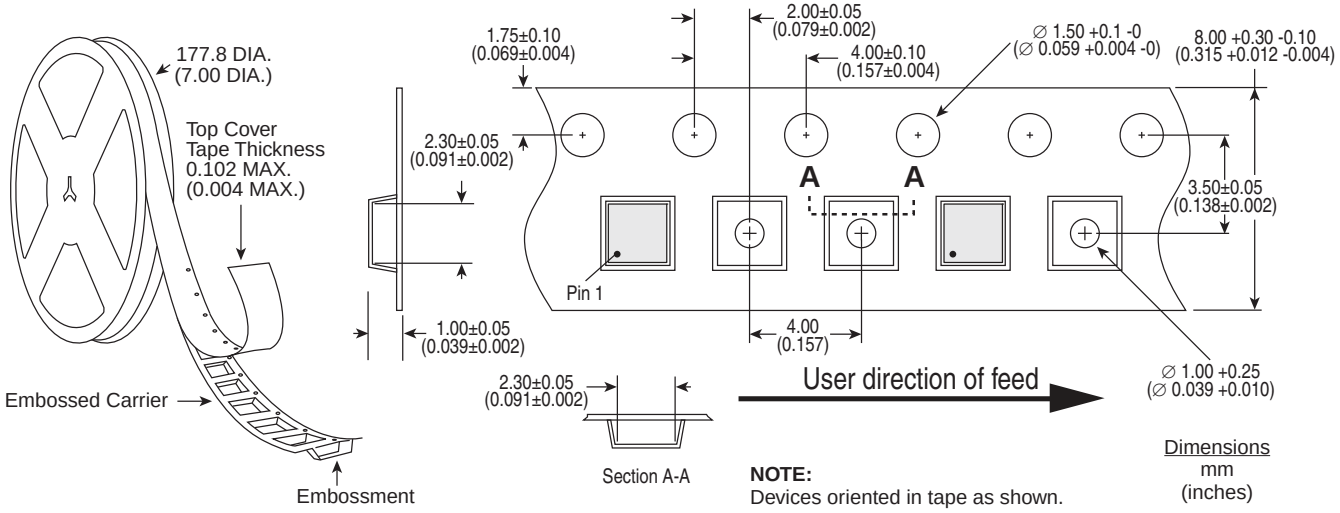
Recommended PCB Land Pattern



Dimensions
mm
(inches)

Note: Dimensions do not include mold or interlead flash, protrusions or gate burrs.

5.5.2 Tape & Reel Specification



NOTE:
Devices oriented in tape as shown.

Dimensions
mm
(inches)

For additional information please visit www.ixysic.com

Specifications: DS-NCD2400M-R01

4/!3/2018

The information below supercedes any previously presented material.

For additional information please visit our website at: https://www.littelfuse.com

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