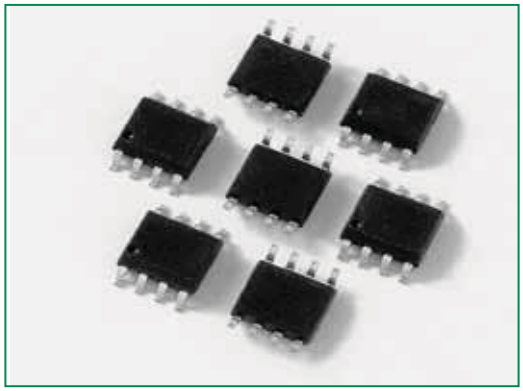
NOT RECOMMENDED FOR NEW DESIGNS

SP4040-02BTG is eventually going to be replaced by the ***SP2502LBTG*** TVS Diode Array with identical form, fit, and function. Please use this device for new or future designs and more detail can be found on Littelfuse.com

SP4040 Series 3.3V 75A Diode Array

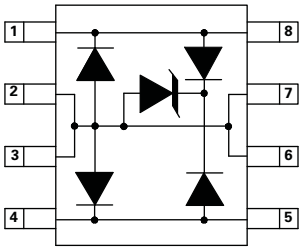
GREEN



Description

The SP4040 provides overvoltage protection for applications such as 10/100/1000 Base-T Ethernet and T3/E3 interfaces. This device has a low capacitance of only 5pF making it suitable for PHY side Ethernet protection and the capability to protect against both longitudinal and differential transients. Furthermore, the SP4040 is rated up to 100A (tp=2/10µs) making it suitable for line side protection as well against lightning transients as defined by GR-1089 (intra-building), ITU, YD/T, etc. The application schematic provides the connection information for a PHY side protection scheme of a single differential pair.

Pinout



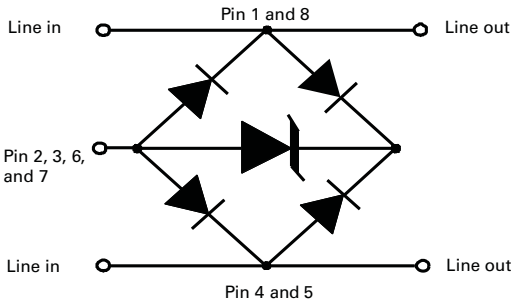
SOIC-8 (Top View)

Note: Pinout diagrams above shown as device footprint on circuit board.

Features

- Lightning protection, IEC61000-4-5, 75A (8/20µs)
- Low clamping voltage
- Low insertion loss, log-linear capacitance
- Combined longitudinal and metallic protection
- Clamping speed of nanoseconds
- SOIC-8 surface mount package (JEDEC MS-012)
- UL 94V-0 epoxy molding
- RoHS compliant

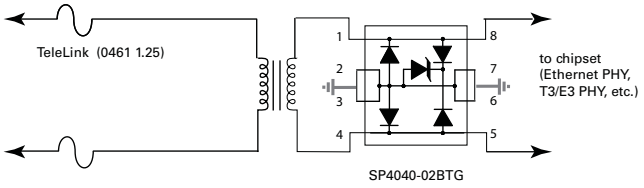
Functional Block Diagram



Applications

- T1/E1 Line cards
- 10/100/1000 BaseT Ethernet
- T3/E3 and DS3 Interfaces
- STS-1 Interfaces

Application Example



The schematic shows protection for a single differential pair as part of a larger high-speed data interface such as Ethernet. The SP4040 provides both metallic (differential) and longitudinal (common mode) protection from lightning induced surge events as specified by regulatory standards such as Telcordia's GR-1089 CORE and ITU K.20 and 21.

The SP4040 protects against both positive and negative induced surge events while the TeleLink fuse provides overcurrent protection for the long term 50/60 Hz power fault events.

Life Support Note:

Not Intended for Use in Life Support or Life Saving Applications

The products shown herein are not designed for use in life sustaining or life saving applications unless otherwise expressly indicated.

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Absolute Maximum Ratings

Parameter	Rating	Units
Peak Pulse Current (8/20µs)	75	A
Peak Pulse Power (8/20µs)	2100	W
IEC 61000-4-2, Direct Discharge, (Level 4)	30	kV
IEC 61000-4-2, Air Discharge, (Level 4)	30	kV
Telcordia GR 1089 (Intra-Building) (2/10µs)	100	A
ITU K.20 (5/310µs)	20	A

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Thermal Information

Parameter	Rating	Units
SOIC Package	170	°C/W
Operating Temperature Range	-55 to 125	°C
Storage Temperature Range	-65 to 150	°C
Maximum Junction Temperature	150	°C
Maximum Lead Temperature (Soldering 20-40s) (SOIC - Lead Tips Only)	260	°C

Electrical Characteristics (T_{OP} = 25°C)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Units
Reverse Stand-Off Voltage	V_{RWM}	I_T≤1µA	-	-	3.3	V
Reverse Breakdown Voltage	V_{BR}	I_T= 2µA	3.3	-	-	V
Snap Back Voltage	V_{SB}	I_T= 50mA	3.3	-	-	V
Reverse Leakage Current	I_R	V_{RWM}= 3.3V	-	-	1	µA
Clamping Voltage, Line-Ground[1]	V_C	I_{PP}= 40A, t_p=8/20 µs	-	-	14	V
Clamping Voltage, Line-Ground[1]	V_C	I_{PP}= 75A, t_p=8/20 µs	-	-	20	V
Clamping Voltage, Line-Ground[1]	V_C	I_{PP}= 100A, t_p=2/10 µs			20	V
Dynamic Resistance, Line-Ground[1]	R_{DYN}	$(V_{C2}-V_{C1})/(I_{PP2}-I_{PP1})$	-	0.2	-	Ω
Clamping Voltage, Line-Line[1]	V_C	I_{PP}= 40A, t_p=8/20 µs	-	-	20	V
Clamping Voltage, Line-Line[1]	V_C	I_{PP}= 75A, t_p=8/20 µs	-	-	30	V
Clamping Voltage, Line-Line[1]	V_C	I_{PP}= 100A, t_p=2/10 µs			30	V
Dynamic Resistance, Line-Line[1]	R_{DYN}	$(V_{C2}-V_{C1})/(I_{PP2}-I_{PP1})$	-	0.3	-	Ω
Junction Capacitance[1]	C_j	Line to Ground V_R=0V, f= 1MHz	-	5	8	pF
		Line to Line, V_R=0V, f= 1MHz	-	2.5	5	pF

[1] Parameter is guaranteed by design and/or device characterization.

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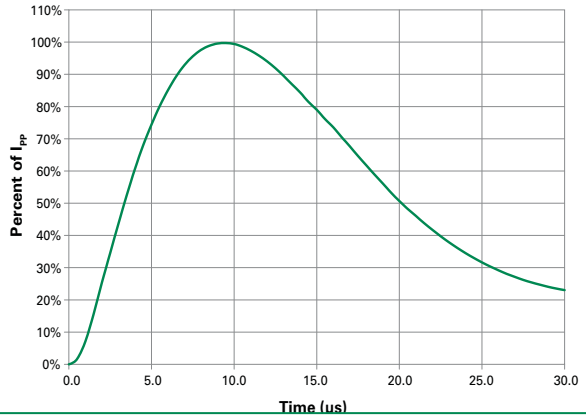
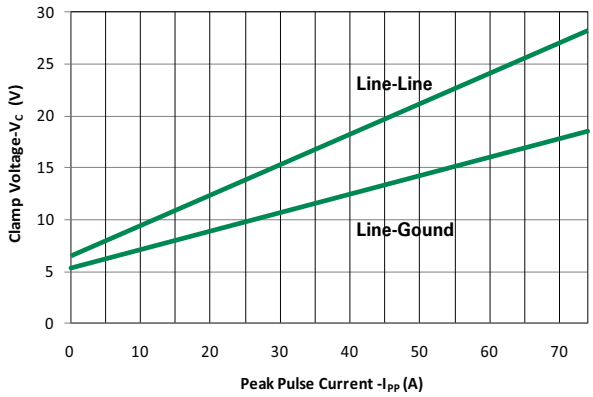
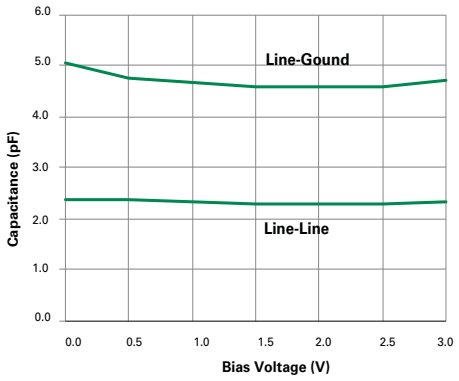
Pulse Waveform



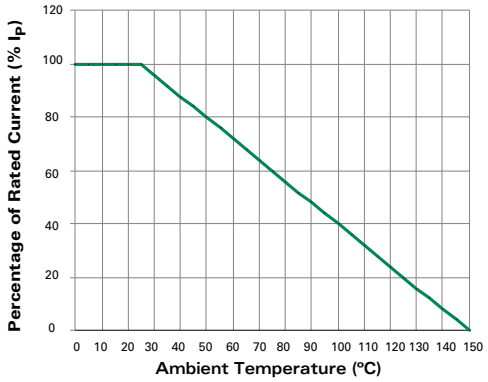
Clamping Voltage vs. I_{PP}



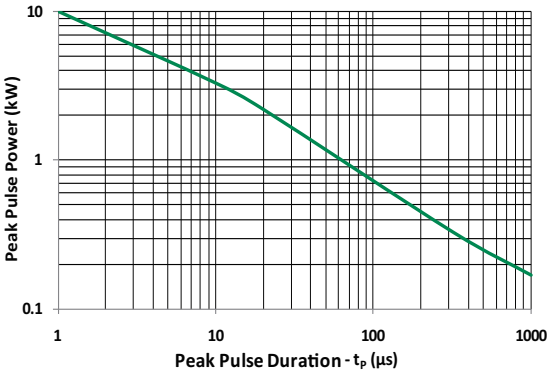
Capacitance vs. Reverse Bias at 1MHz



Current Derating Curve

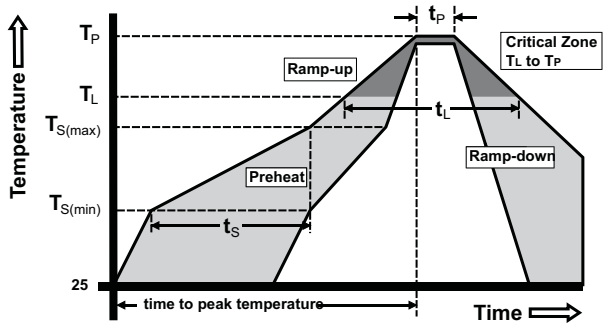


Non-Repetitive Peak Pulse Power vs. Pulse Time



Soldering Parameters

Reflow Condition		Pb – Free assembly
Pre Heat	-Temperature Min ($T_{s(min)}$)	150°C
	-Temperature Max ($T_{s(max)}$)	200°C
	-Time (min to max) (t_s)	60 – 180 secs
Average ramp up rate (Liquidus) Temp (T_L) to peak		3°C/second max
$T_{S(max)}$ to T_L - Ramp-up Rate		3°C/second max
Reflow	-Temperature (T_L) (Liquidus)	217°C
	-Temperature (t_L)	60 – 150 seconds
Peak Temperature (T_P)		$260^{+0/-5}$ °C
Time within 5°C of actual peak Temperature (t_p)		20 – 40 seconds
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.
Do not exceed		260°C



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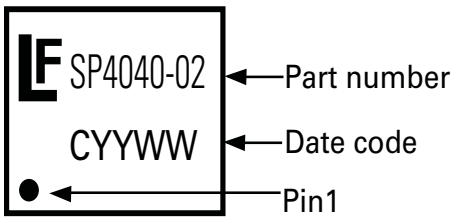
Part Marking System



Product Characteristics

Lead Plating	Matte Tin plating
Lead Material	Copper Alloy
Lead Coplanarity	0.0004 inches (0.102mm)
Substitute Material	Silicon
Body Material	Molded Epoxy
Flammability	UL 94 V-0

Notes :
1. All dimensions are in millimeters
2. Dimensions include solder plating.
3. Dimensions are exclusive of mold flash & metal burr.
4. Blo is facing up for mold and facing down for trim/form, i.e. reverse trim/form.
5. Package surface matte finish VDI 11-13.

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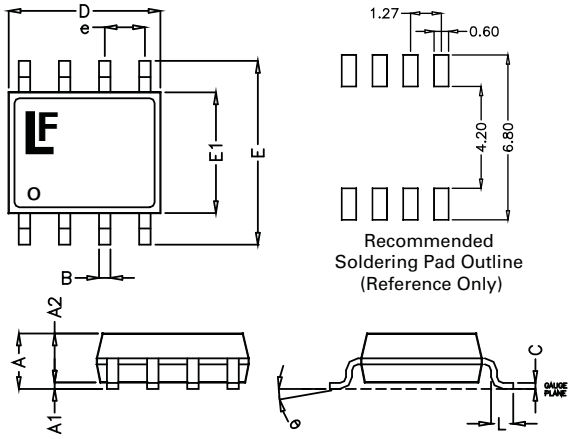
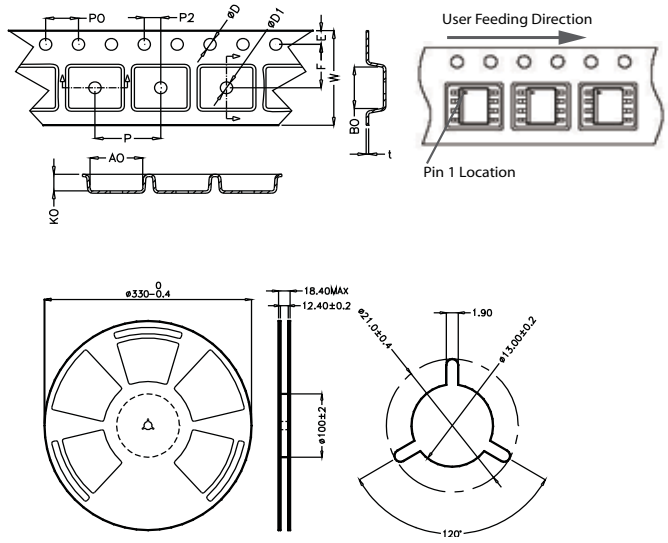
Package Dimensions — Mechanical Drawings and Recommended Solder Pad Outline



Package	SOIC			
Pins	8			
JEDEC	MS-012			
	Millimetres		Inches	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A1	0.10	0.25	0.004	0.010
A2	1.25	1.65	0.050	0.065
B	0.31	0.51	0.012	0.020
c	0.17	0.25	0.007	0.010
D	4.80	5.00	0.189	0.197
E	5.80	6.20	0.228	0.244
E1	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
L	0.40	1.27	0.016	0.050

Embossed Carrier Tape & Reel Specification — SOIC Package



	Millimetres		Inches	
	Min	Max	Min	Max
E	1.65	1.85	0.065	0.073
F	5.4	5.6	0.213	0.22
P2	1.95	2.05	0.077	0.081
D	1.5	1.6	0.059	0.063
D1	1.50 Min		0.059 Min	
P0	3.9	4.1	0.154	0.161
10P0	40.0 +/- 0.20		1.574 +/- 0.008	
W	11.9	12.1	0.468	0.476
P	7.9	8.1	0.311	0.319
A0	6.3	6.5	0.248	0.256
B0	5.1	5.3	0.2	0.209
K0	2	2.2	0.079	0.087
t	0.30 +/- 0.05		0.012 +/- 0.002	

Part Numbering System

SP 4040 - 02 B T G

- SP: Silicon Protection Array
- 4040: Series
- 02: Number of Channels
- B: Package B = SOIC-8
- T: T= Tape & Reel
- G: G= Green

Ordering Information

Part Number	Package	Marking	Min. Order Qty.
SP4040-02BTG	SOIC-8	SP4040-02	2500