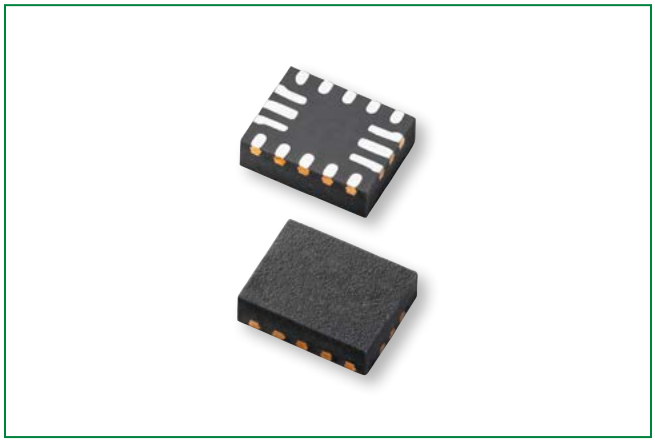
LS24062RQ23

24V 6A Bidirectional eFuse with Dual Port Independent Current Limit Setting



Web Resources

Download ECAD models, order samples, and find technical recources at www.littelfuse.com

Agency Approvals

Agency	Agency File/Certificate Number
c UL us	E528847

Description

The LS24062RQ23 is an advanced 24V 6A rated bidirectional load switch which provides overload, short circuit, input voltage surge, excessive inrush current and over-temperature protections to power the system. The built-in 24mΩ ultra low RDS(ON) power switch helps reducing power loss during normal operation. The device features two input/output ports, VBUS1 and VBUS2, which are rated at 30V Absolute Maximum. Each port has independent enable, external current limit setting and discharge control pins. The integrated two N-channel power switch M1 and M2 in-series configuration blocks any leakage between VBUS1 and VBUS2 two ports when the device is disabled. The LS24062RQ23 is available in low profile 16 leads QFN 2.5mm x 3.2mm package.

Features and Benefits

- Wide Supply Voltage Range from 3V to 24V
- 30V Tolerance on Port VBUS1 and VBUS2
- Integrate a 24mΩ Ultra Low On Protection Switch
- External Adjustable Soft-Start Time
- External Adjustable Input Over-voltage Threshold
- Short-circuit Protection
- Fault Indicator
- Thermal Shutdown Protection and Auto Recovery
- Each Port VBUS1/VBUS2 Independent Control
- External Adjustable Current Limit
- Enable Interface Pin
- Port Discharge Interface Pin
- QFN 2.5mm×3.2mm_16L Packages
- Pb-Free and RoHS Compliant
- UL Recognized to UL 62368-1

Applications

- Notebook, Desktop, Servers and Tablets
- Dongle and Docking Stations
- Power Accessories
- USB-PD ports in various applications

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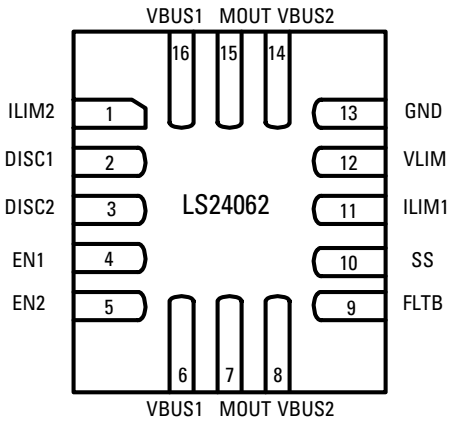
Pinout Designation



Pin #	Pin Name	Description
1	ILIM2	Port VBUS2 current limit program pin. Program the current limit of power switch M2 (VBUS2 to MOUT) by connecting a resister from ILIMT2 to ground. ILIM2 pin can't be shorted to GND. If the system requires a single component fail safe, use 2 resistor in series to program current limit.
2	DISC1	Port VBUS1 discharge control input. Pull Logic High discharges port VBUS1 to GND through an internal 190Ω pull down resistor.
3	DISC2	Port VBUS2 discharge control input. Pull Logic High discharges port VBUS2 to GND through an internal 190Ω pull down resistor.
4	EN1	Enable control input of the power switch M1 (VBUS1 to MOUT). Pull Logic High enables power switch M1, and pull Logic Low disables the power switch M1. This pin has a pull-down resistor of typically 1MΩ when the device is disabled. See Table 1 EN1 and EN2 Control Sequence.
5	EN2	Enable control input of the power switch M2 (VBUS2 to MOUT). Pull Logic High enables power switch M2 and pull Logic Low disables the power switch M2. This pin has a pull-down resistor of typically 1MΩ when the device is disabled. See Table 1 EN1 and EN2 Control Sequence.
6,16	VBUS1	Bidirectional Input/Output Port 1. Connect VBUS1 to power supply input or output to the load.
7,15	MOUT	The N-type power switch M1 and M2 common drain output pin. Leave this pin float if it is not used. Although MOUT pin can provide power to the other circuitry when EN1 or EN2 pin is pulled Logic High, need to pay extra attention when use it. MOUT pin does NOT have short circuit protection due to the power switch M1 and M2 body diode, and the current drawn from MOUT pin also affects current limit setting accuracy at ILIM1 or ILIM2 pin. See Application Notes how to take power from the MOUT pin.
8,14	VBUS2	Bidirectional Input/Output Port 2. Connect VBUS2 to power supply input or output to the load.
9	FLTB	Fault event indicator open drain output pin. A pull-up resistor is connected from FLTB pin to any voltage less than 28V. Active Low indicates input over-voltage, over-current and over-temperature fault events.
10	SS	Soft-start time program pin. Connect a capacitor to ground to program the soft start time.
11	ILIM1	Port VBUS1 current limit program pin. Program the current limit of switch M1 (VBUS1 to MOUT) by connecting a resister from ILIMT1 to ground. ILIM1 pin can't be shorted to GND. If the system requires a single component fail safe, use 2 resistor in series to program current limit.
12	VLIM	VBUS1 or VBUS2 Input over voltage protection threshold set pin. Program input over-voltage protection threshold (VOVP) by connecting a resister to ground. Typical VOVP=12x10μAxRVLIM. Recommend to set input over-voltage protection threshold range 5V to 24V.
13	GND	Ground pin.

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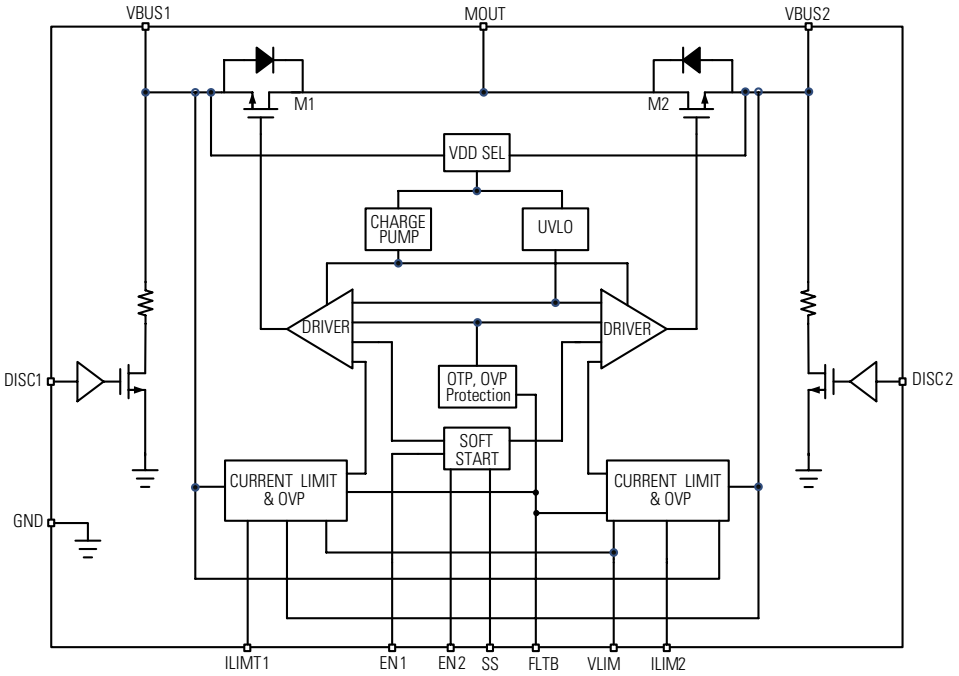
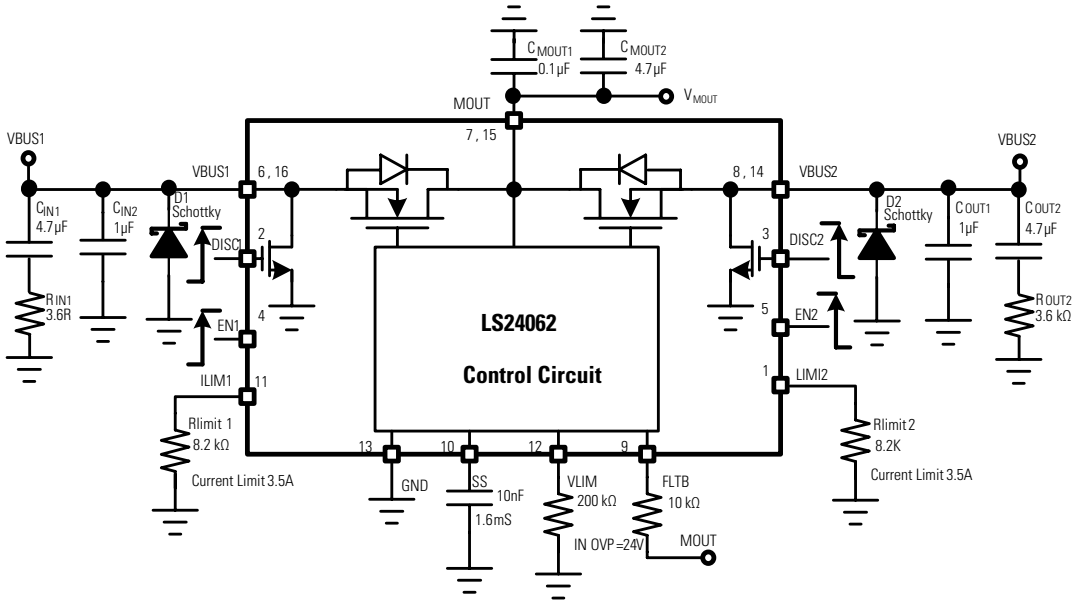
Functional Block Diagram



Typical Application (For USB Type-C PD Application)



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EN1 and EN2 Control Power-On Sequences

EN1	EN2	Current Flow Direction	The Power Switch M1 and M2 States	
			VBUS1 to MOUT M1	VBUS2 to MOUT M2
Hi	Lo	VBUS1to MOUT	ON	OFF
Lo	Hi	VBUS2 to MOUT	OFF	ON
Hi	Hi	EN1 Pulls Logic Hi First, VBUS1 to VBUS2	ON	ON
		EN2 Pulls Logic Hi First, VBUS2 to VBUS1		
Lo	Lo	Shutdown mode, no current flowing between VBUS1 and VBUS2. Not to recommend drawing current from MOUT pin through the power switch M1 or M2 body diode in the shutdown mode.	OFF	OFF

Absolute Maximum Ratings

Parameter	Value	Unit
VBUS1, VBUS2 and MOUT to GND	-0.3~+30	V
VBUS1 to VBUS2	-30~+30	V
EN1, EN2 and FLTB to GND	-0.3~+28	V
The other pins to GND	-0.3~+6.5	V
Pulsed Switch Current (<100us, Note 2 and 3)	20	A
ESD, Human Body Model (HBM)	±2000	V
Lead Temperature (Soldering 10s)	+260	°C
Junction Temperature Range	-40 to +150	°C
Storage Temperature Range	-65 to +150	°C

Notes:

1. Stress exceeding those listed "Absolute Maximum Ratings" may damage the device.
2. The maximum continuous current rating is limited by the package power dissipation.
3. Single pulse current width is limited by the maximum junction temperature T_J_MAX=+150°C.

Thermal information

Symbol	Value	Units
Maximum Power Dissipation (T_A=25°C)	1.8	W
Thermal Resistance (θ_{JA})	55.12	°C/W
Thermal Resistance (θ_{JC})	15.6	°C/W

Note:

1. Measured on JESD51-7, 4-Layer PCB.
2. The maximum allowable power dissipation is a function of the maximum junction temperature T_{J_MAX}, the junction to ambient thermal resistance θ_{JA}, and the ambient temperature TA. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\_MAX}=(T_{J\_MAX}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Recommend Operating Conditions

Symbol	Value	Units
VBUS1, VBUS2 and FLTB	+3 to +24	V
Continuous Switch Current	6	A
EN1 and EN2	-0.3~24	V
DISC1 and DISC2	-0.3~5.5	V
Junction Temperature Range	-40 to +125	°C

Notes: The device is not guaranteed to function outside of the recommended operating conditions.

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Electrical Characteristics

T_A = +25°C, VBUS1=5V, R_{ILIM1}= R_{ILIM2}=5.1kΩ, R_{VLIM}=200kΩ and C_{VBUS1}=C_{VBUS2}=C_{MOUT}=0.1μF, unless otherwise specified (Note 1).

Symbol	Parameter	Test Conditions	Min	Nom	Max	Unit
V_{BUS1}	Input Voltage Range	VBUS1 is input, and VBUS2 is output	3		24	V
V_{BUS2}		VBUS2 is input and VBUS1 is output	3		24	
I_Q	Quiescent Current	VBUS1=5V~24V, V_{EN1}=5V, V_{EN2}=0V/5V		450	600	μA
		VBUS2=5V~24V, V_{EN2}=5V, V_{EN1}=0V/5V		450	600	
I_{SHDN}	Shutdown Current	VBUS1=5V~24V, V_{EN1}= V_{EN2}=0V		10	20	μA
		VBUS2=5V~24V, V_{EN1}= V_{EN2}=0V		10	20	
$V_{EN1/2\_ON}$	EN1/2 Turn-on Threshold	EN1/EN2 Rising	1.5		24	V
$V_{EN1/2\_OFF}$	EN1/2 Turn-off Threshold	EN1/EN2 Falling			0.4	V
T_{Delay}	EN1_HtoL to EN2_LtoH Transition Delay Time (Note 2)	EN1 Falling to EN2 Rising	5			msec
T_{Delay}	EN2_HtoL to EN1_LtoH Transition Delay Time (Note 2)	EN2 Falling to EN1 Rising	5			msec
$R_{EN1/2PD}$	EN1/2 Pull Down Resistance			1	-	MΩ
V_{UVLO}	Input UVLO Threshold	VBUS1 is input and VBUS2 is output VBUS1 Rising		2.95		V
		VBUS2 is input, and VBUS1 is output VBUS2 Rising		2.95		
V_{HYS}	Input UVLO Hysteresis	VBUS1 is input, VBUS1Falling		450		mV
		VBUS2 is input, VBUS2Falling		450		
t_{pwrdly}	Power On Delay Time	VBUS1 is input, V_{EN1}=V_{EN2}=0 to high		500		μS
		VBUS2 is input, V_{EN1}=V_{EN2}=0 to high		500		
$R_{DS(ON)}$	VBUS1 to VBUS2 Power Switch On Resistance	VBUS1/VBUS2=5V~24V		24	40	μS
I_{LKG_SW}	Power Switch Leakage Current	V_{MOUT}=24V, V_{VBUS1}=V_{VBUS2}=0V V_{EN1}=V_{EN2}=0V			10	μA
$K_{ILIM1/2}$	Current Limit ILIM1/2 Setting Factor	$I_{ILIM1/2}$=1A~6A		28		A*kΩ
$I_{LIM1/2}$	Current Limit	$R_{ILMT1/2}$=28 kΩ	0.9	1	1.1	A
		$R_{ILMT1/2}$=9.33 kΩ	2.7	3	3.3	
		$R_{ILMT1/2}$=5.6kΩ	4.5	5	5.5	
K_{OVP}	VBUS1/VBUS2 Input Over-voltage Protection (OVP) Threshold VLIM Setting Factor	V_{OVP} =K_{OVP}*R_{VLIM} V_{OVP}=5V~24V		120		mV/KΩ
I_{VLIM}	VLIM Source Current			10		μA
V_{OVP}	VBUS1/VBUS2 Input Over-voltage Protection(OVP) threshold	VBUS1 is input, VBUS1 Rising R_{VILIM}=50K		6		V
		VBUS2 is input, VBUS2 Rising, R_{VILIM}=50K				
		VBUS1 is input, VBUS1 Rising, R_{VILIM}=200K	21	24	27	
		VBUS2 is input, VBUS2 Rising, R_{VILIM}=200K				
V_{OVPHYS}	VBUS1/VBUS2 Input Over-voltage Protection(OVP) Threshold Hysteresis	VBUS1 is input, VBUS1 Falling R_{VILIM}=50K		0.7		V
		VBUS2 is input, VBUS2 Falling, R_{VILIM}=50K				
		VBUS1 is input, VBUS1 Falling R_{VILIM}=200K		0.7		
		VBUS2 is input, VBUS2 Falling, R_{VILIM}=200K				

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Symbol	Parameter	Test Conditions	Min	Nom	Max	Unit
T_{SS}	Soft-start Time	C_{SS}=100nF		16.7		msec
		SS Floating		0.8		
I_{SS}	SS Source Current	V_{SS}=0V		2.5		μA
V_{FOL}	FLTB Output Low Voltage	Fault Event, I_{FLTB}=1mA			350	mV
I_{Flkg}	FLTB Leakage Current	No Fault Event, V_{FLTB}=24V		0.01	1	μA
$T_{FLTBDLY1}$	FLTB Delay Time	Enter Current Limit or Short Circuit Fault Event, Pull FLTB Low		3		msec
$T_{FLTBDLY2}$	FLTB Release Delay time	Exit Fault Event, Release FLTB HiZ		1.5		msec
R_{DISC}	VBUS1/VBUS2, Discharge resistance	EN1=Hi or EN2=Hi, DISCx=Hi		350		Ω
V_{DISC_ON}	DISC1/2 Logic High Threshold	DISC1/DISC2 Rising	1.5		5	V
V_{DISC_OFF}	DISC1/2 Logic Low Threshold	DISC1/DISC2 Falling			0.4	V
I_{DISLKG}	DISC1/2 Input Leakage Current	$V_{DISC1/DSIC2}$=0V	-1		1	μA
I_{DISLKG}	DISC1/2 Input Leakage Current	$V_{DISC1/DSIC2}$=5V		6	9	μA
T_{SD}	Thermal Shutdown Temperature			150		°C
T_{HYS}	Thermal Shutdown Hysteresis			25		°C

Note:

1: Limits are 100% production testes @T_A=+25°C, unless otherwise noted. Limits over the temperature range are guaranteed by design.

2: Guaranteed by design.

Figure 1. Quiescent Current Vs. Input Voltage

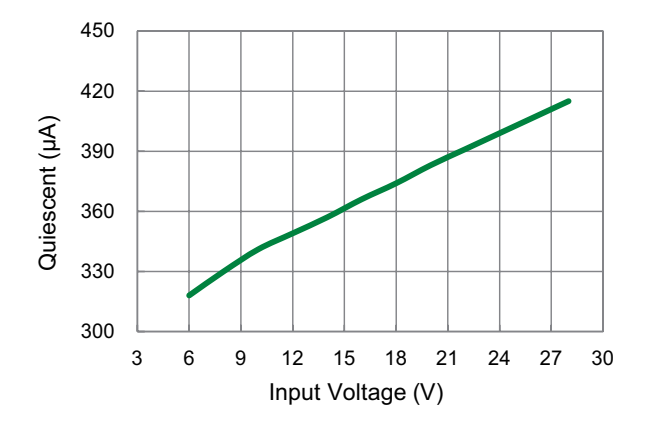

Figure 2. Current Limit Vs. RILIM Resistor Value

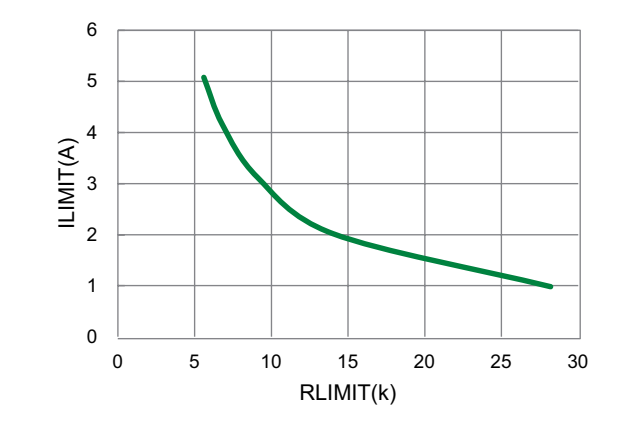

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Figure 3. Programmable Soft-Start Time (V_{BUS1} on, C_{SS}=10nF)

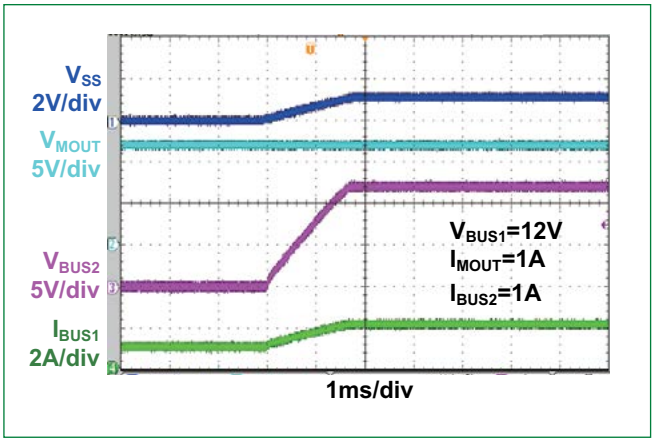

Figure 4. Programmable Soft-Start Tim (V_{BUS2} on, C_{SS}=10nF)

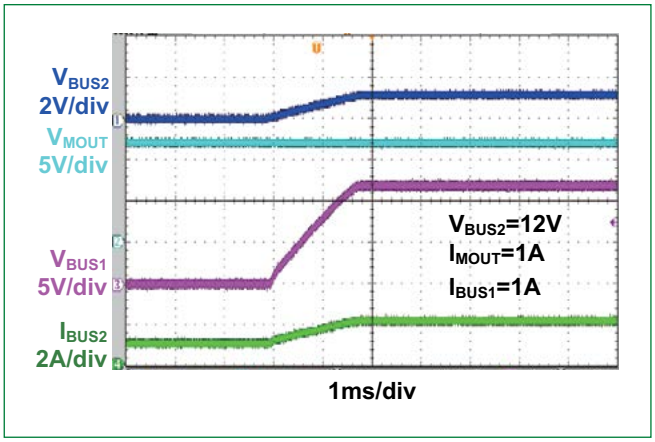

Figure 5. Input Over Voltage Protection (V_{VBUS1} on, R_{VLIM}=120kΩ)

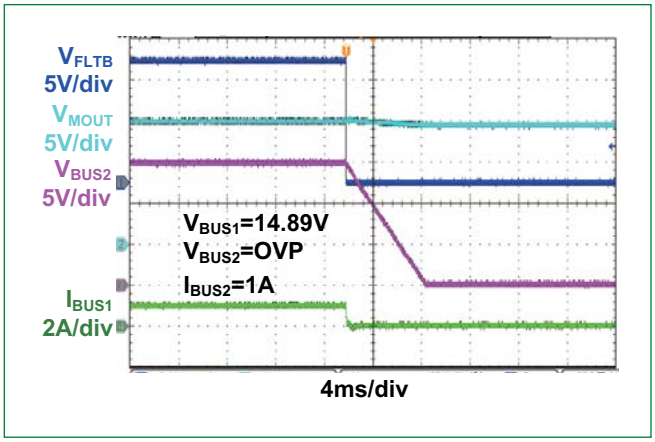

Figure 6. Input Over Voltage Protection (V_{VBUS2} on, R_{VLIM}=120kΩ)

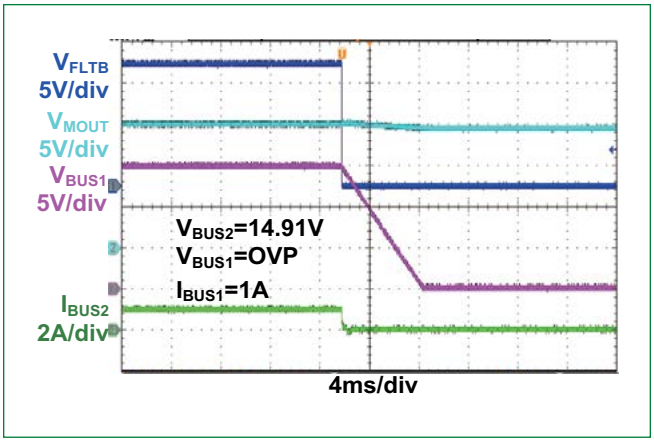

Figure 7. VBUS1 Discharge(DISC1)

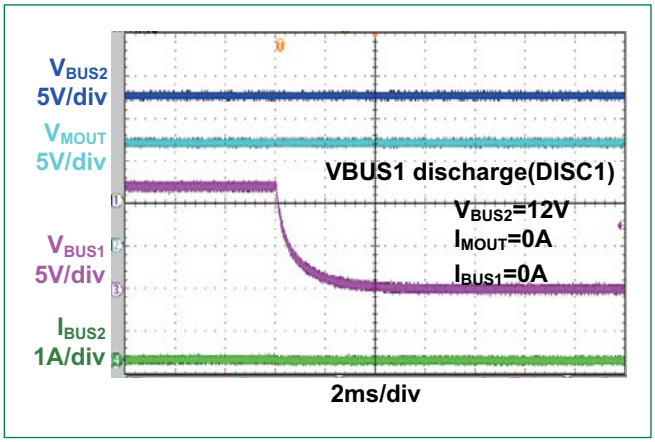

Figure 8. VBUS2 Discharge(DISC2)

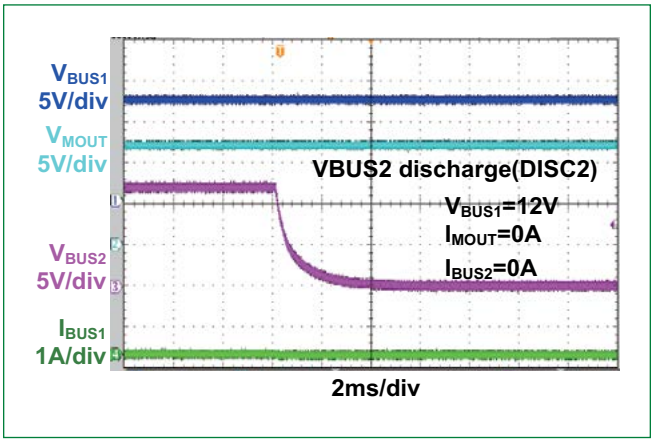

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Figure 9. VBUS1 Short Circuit Protection

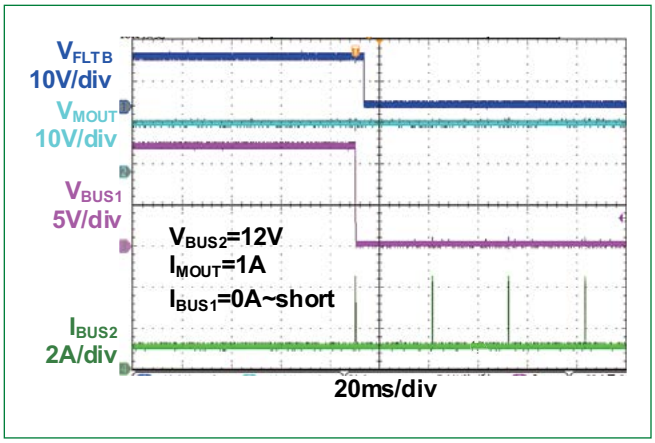


Figure 10. VBUS1 Short Circuit Protection Recovery

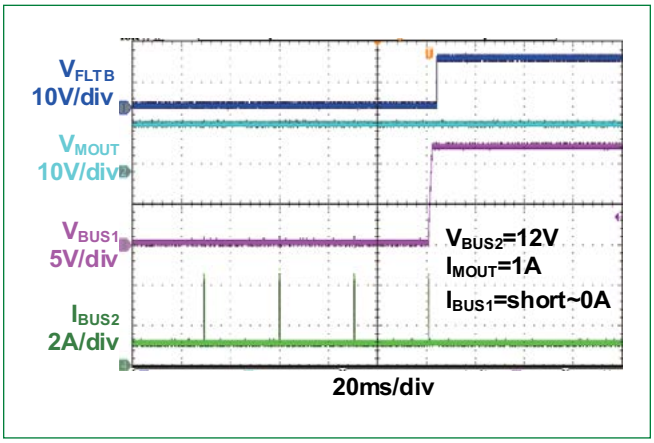


Figure 11. VBUS2 Short Circuit Protection

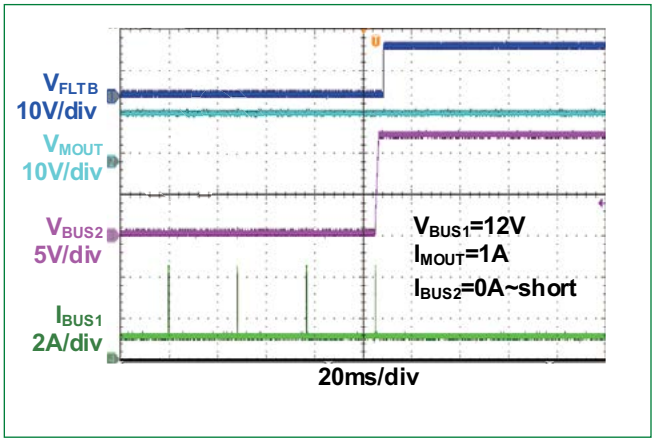
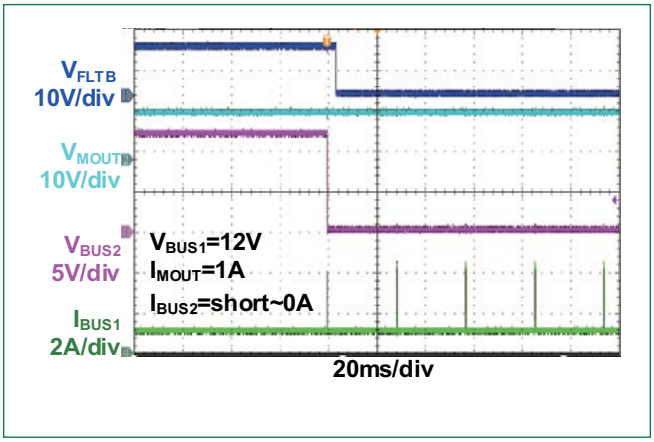


Figure 12. VBUS2 Short Circuit Protection Recovery



Detailed Description

The LS24062RQ23 is an advanced bidirectional power switch with adjustable soft-start, adjustable current limit threshold, input under-voltage, adjustable input over-voltage, over-temperature and short circuit protections. The device features two input/output ports, VBUS1 and VBUS2, which are rated at 30V Absolute Maximum. Each port has independent enable, input over-voltage protection (OVP), external current limit setting and discharge functions. The device integrates two N-channel power switch M1 and M2 in series with a common drain output MOUT. When both EN1 and EN2 pin are pulled low, the device is in shutdown mode and turns off both power switch M1 and M2 to prevent current flowing between port VBUS1 and VBUS2. Users control EN1 and EN2 on sequence to set power switch M1 and M2 states and current flow direction. Refer to Table 1 EN1 and EN2 Power-On Sequence. The output voltage ramp up time is controlled by either the internal 0.8msec soft-start or external programmable soft-start with a capacitor between SS pin and GND. After a successful start-up sequence, the device actively monitors each power switch current to ensure that the overload current limit IILMT1/2 programmed by pin ILIM1/2 ILIM2 is not exceeded. The device monitors input voltage and turns off the power switch if the input voltage spike exceeds the input over-voltage threshold which is set by pin VLIM. Both current limit and input over-voltage protection keep the output device safe from the harmful input voltage and current transients. The device has a built-in thermal sensor. If the device junction temperature (T_J) exceeds the thermal regulation point +125°C, the current limit will be decreased until T_J is regulated around +125°C. In some deadly output short circuit events, and the device junction temperature (T_J) quickly rises and exceeds the thermal shutdown threshold T_{SD}, typically +150°C, the device will shut down two power switch M1 and M2 immediately to disconnect the load from the input supply. The LS24062RQ23 remains off during a cooling period until the junction temperature falls below T_{SD} -25°C, after the device will attempt to restart.

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Application Information

Input/Output Bidirectional Port VBUS1/VBUS2

The LS24062RQ23 operates as a bidirectional switch which allows current flow either VBUS1 to VBUS2 or VBUS2 to VBUS1 depending on EN1/EN2 control sequence. VBUS1 or VBUS2 can be connected to the Adapter input power supply or output to periphery. The device automatically selects power from either VBUS1 or VBUS2 whichever is higher. The recommended VBUS1/VBUS2 input voltage range is 3V to 24V with 28V transient tolerance. Place a high quality 0.1µF in parallel with at least 22µFx2 or higher ceramic type X5R or X7R bypass capacitor at the VBUS1/VBUS2 pin to ground GND for proper decoupling. The capacitor voltage rating should exceed the maximum input voltage range. In the event of the short circuit with a long cable, the cable parasitic inductance and the output ceramic forms high Q LC-Tank. The short circuit high current slew rate di/dT may cause the port VBUS1/VBUS2 pin going negative voltage up to -10V. The VBUS1/VBUS2 pin negative voltage spike triggers ON the pin ESD diode and put voltage stress on the internal power switch. If the voltage difference between VBUS1 pin and VBUS2 pin exceeds 28V, the power switch will be permanently damaged. In order to limit VBUS1/VBUS2 pin negative voltage spike in the short circuit event, recommend to add an additional 470µF Electrolytic capacitor in parallel with output ceramic capacitors. Due to high ESR value of Electrolytic capacitor, the output parasitic L-C tank Q is damped.

USB Type-C Cable Short Circuit Protection

The VBUS1/VBUS2 pin of the LS24062RQ23 is connected to USB Type-C cable VBUS pin. When a USB cable is hot plugged in/out of the USB Type-C connector, large ground current could be seen at the VBUS pin. When the far end of a connected cable is short to ground for whatever reason, the OUT pin of the LS24062RQ23 could also see a large ground current. The large ground current with high slew rate di/dt can cause the LS24062RQ23 OUT pin going negative voltage up to -10V due to the USB Type-C cable parasitic inductance. The excessive negative voltage spike will trigger on the LS24062RQ23 internal OUT pin ESD diode and put voltage stress on the internal power switch. If the voltage difference between LS24062RQ23 IN pin and OUT pin exceeds 28V, the power switch will be permanently damaged. Recommend to place a Schottky diode as close as possible to LS24062RQ23's VBUS1 and VBUS2 pin to help absorb large GND current which may result in LS24062RQ23 false operation. Another method of clamping the VBUS negative voltage spike is to use a RC snubber. The RC snubber modifies the characteristic of total RLC response in the USB Type-C cable hot-plug from being under-damped to critically-damped or over-damped in the USB cable hot-plug. The RC snubber actually changes the hot-plug response, so the voltage on VBUS does not ring and the voltage is limited. However, the USB Type-C and Power Delivery specifications limit the range of capacitance that can be used on VBUS for the RC snubber. VBUS capacitance must have a minimum 1µF and a maximum of 10µF. The RC snubber values chosen support up to 4meter USB Type-C cable (maximum length allowed in the USB Type-C specification) being hot plugged, is to use 4.7µF capacitor in series with a 3.6-Ω resistor. In parallel with the RC snubber a 1µF capacitor is used, which always ensures the minimum USB Type-C VBUS capacitance specification is met. This VBUS1/VBUS2 clamping circuit is shown below in Figure 1.

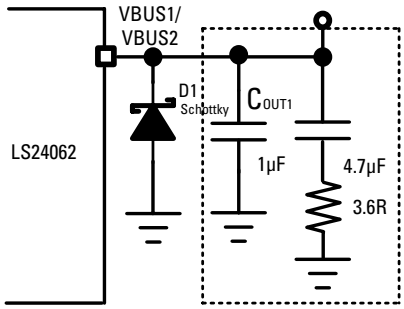

Figure 13. Clamp USB Type-C VBUS overshoot/undershoot with a Schottky Diode and RC Snubber

EN1 (V_{EN}1) and EN2 (V_{EN}2) Enable Control

Enable interface pin EN1/EN2 has ON/OFF threshold of 1.5V (Min) and 0.4V (Max) respectively. EN1 controls the power switch M1 (VBUS1 to MOUT), and EN2 controls the power switch M2 (VBUS2 to MOUT). Pull both EN1 and EN2 pin low below OFF threshold (<0.4V) to disable the power switch and all protection circuits, and the device is in the low power shutdown mode and draws only 10µA current from the input supply. There is an internal 1MegΩ pull-down resistor to ensure the power switch OFF if EN1/EN2 pin is floated. EN1/EN2 pin can tolerate maximum 28V voltage spike. EN1 and EN2 set power on sequence and current flow direction shown in the Table 1. To ensure correct power switch turning on sequence, keep EN1_HtoL to EN2_LtoH transition delay1 time ≥5ms; and EN2_HtoL to EN1_LtoH transition delay2 time ≥5ms as shown in Figure2 below.

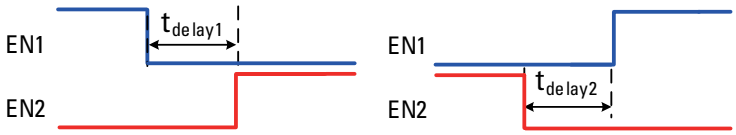

Figure 2. EN1 and EN2 Timing Control Diagram

Over-voltage Protection (OVP)

The LS24062RQ23 constantly monitors the supply voltage of VBUS1 and VBUS2, and it disables the power switch and pulls FLTB pin LOW to report the fault condition in case voltage on VBUS1 or VBUS2 exceeding the external programmed the over-voltage protection threshold VOVP. Once the VBUS1 and VBUS2 voltage drops below input over-voltage threshold V_{OVP} and no other protection circuit is active, the power switch resumes ON.

An external resistor R_{VLIM} is connected from VLIM pin to GND to set the over-voltage protection threshold V_{OVP}. The device sources typical 10µA to VLIM pin. The voltage drop V_{VLIM} across the RVLIM resistor externally adjusts the over-voltage threshold from 5V to 24V using Equation (1):

$$V_{OVP} = K_{OVP} \times V_{VLIM} = 12 \times 10\,\mu A \times R_{VLIM} \quad \text{.....(1)}$$

The recommended input over-voltage threshold setting is shown in the Table 1.

R_{VLIM} (kΩ)	45.8	82.5	137.5	183.3	200
Input Over-voltage Threshold (V)	5.5	9.9	16.5	22	24

Over-voltage Protection Threshold Setting by an External Resistor R_{VLIM}

Soft Start

When EN1 and EN2 are asserted high, the soft start control circuitry controls the gate voltage of the power switch in a manner such that the output voltage is ramped up linearly until it reaches input voltage level during power on. The in-rush current at power-on is limited by the regulated output voltage ramp up rate through the soft-start time. The built-in internal soft-start time is typical 0.8msec. If users prefer the soft-start time longer than 0.8msec, connect an external capacitor CSS between SS pin and ground to re-adjust the soft-start time. The external soft-start time is approximately calculated by Equation (2):

$$T_{SS} = C_{SS} \times 1.67 \times 10^5 \quad \text{.....(2)}$$

The recommended soft-start time setting is shown in the Table 2.

CSS Value (nF)	None or < 4.7nF	10	33	47	100
Soft-start Time TSS (msec)	0.8	1.6	5.5	7.8	16.7

Soft-start Time Setting by An External Capacitor CSS

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Current Limit ILIM1/ILIM2

For current limited adaptors or power sources, users can program the input current limit level to prevent the load current overload the source. The LS24062RQ23 different current direction current limit is independently set with external resistors connected between ILIM1/ ILIM2 and GND. The power switch M1 (VBUS1 to MOUT) current limit is programmed by the ILIM1 resistor RILIM1, and the power switch M2(VBUS2 to MOUT) is programmed by the ILIM2 resistor RILIM2. If over-load occurs, the internal circuitry limits the current based on the value of RILIM½ and pulls FLTB pin LOW to report the fault condition. ILIM1 or ILIM2 pin can't be short to GND. If the system requires a single component fail safe, use 2 resistor in series to program input current limit. The current limit resistor RILIM is selected with Equation (3).

$$R_{ILIM\ 1/2} = \frac{K_{\ ILIM}}{I_{ILIM\ 1/2}} = \frac{28\ A * k\Omega}{I_{\ ILIM}\ 1/2} \quad \text{.....(3)}$$

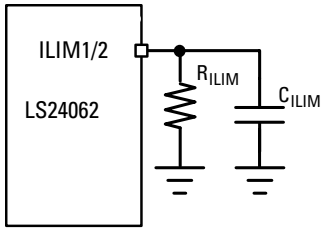
The common current limit threshold setting is shown in the Table 3.

R_{ILIM} (kΩ)	28	14	9.33	7	5.6	4.6
Current Limit I_{ILIM} (A)	1.0	2.0	3.0	4.0	5.0	6.0

Current Limit Setting by an External Resistor R_{ILIM}

System design need to select output capacitor so that during start-up, load current plus output capacitor charging current should not exceed set current limit, otherwise it might trigger current limit and cause restart.

In applications where high output capacitance is required or there might be short pulses of high load current which exceed the set current limit, a capacitor CILIM can be placed in parallel with RLIM. CILIM will provide a delay for over current triggering so the load switch can pass high current during this delay time. To be noticed though, during the delay time, LS24062RQ23 internal current limit is still activated. Care should be taken to prevent switch current exceed this limit.



Short Circuit Protection

The LS24062RQ23 integrates a fast-trip comparator to quickly turn off the power switch when VBUS1 or VBUS2 is shorted to ground. The device operates hiccup mode in short circuit protection. Once the short circuit fault is detected, the power switch is turned off and is forced off for a given time. At the end of the predetermined time, a restart attempt is made by soft-starting the power switch. If the over-load condition has been removed, the power switch will turn on and operate normally; otherwise, the device will see another over-current event and shut off the power switch again, repeating the previous cycle. The excess heat due to overload lasts for only a short duration in the hiccup cycle, hence the junction temperature of the power devices is much lower.

Thermal Foldback and Thermal Shutdown Protection

The LS24062RQ23 continuously monitors the current and keeps it limited to the value programmed by R_{ILIM1}/ R_{ILIM2}. In the normal operation or current limit protection mode, If power dissipation in the internal MOSFET PD = $|V_{VBUS1} - V_{VBUS2}| \times I_{LOAD}$ is too high, LS24062RQ23 will engage thermal foldback to reduce the current limit value so that the junction temperature (T_J) is maintained around +125°C. Figure 4. shows thermal foldback current limit. In some deadly output short circuit events, the output voltage drops with current limit I_{ILIM1}/ I_{ILIM2}. It will result in the increasing junction temperature T_J with the increased power consumption and the device junction temperature (T_J) quickly rises and exceeds the thermal shutdown threshold T_{SD}, typically +150°C, the device will shut down the power switch and disconnect the load from the supply. The LS24062RQ23 remains off during a cooling period until the junction temperature falls below T_{SD} -20°C, after the device will attempt to restart.

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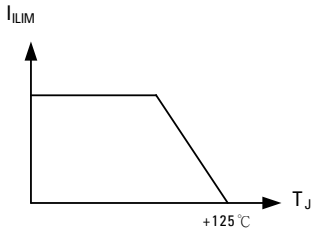


Figure 14. Thermal Foldback Current Limit

Fault Indicator FLTB

The FLTB is an open-drain output that requires an external pull-up resistor connected to any voltage less than 28V. The pull up resistor value is recommended to be 10kΩto 1000kΩ. FLTB pin indicates the state of the power switch. When no fault is detected and power switch is conducting, FLTB stays at high impedance HiZ. The device generates a warning flag and FLTB output low whenever one of the following fault event occurs: VBUS1/ VBUS2 over-voltage, over current limit, short circuit and over-temperature. And FLTB output change to be low with typical 3msec de-glitch time when over current or short circuit event occurs. The FLTB signal remains at 'low' until the device exits from the fault events with typical 1.5msec de-glitch time.

VBUS1/VBUS2 Port Discharge Function

The port VBUS1 discharge function is controlled by an external control input DISC1, and the port VBUS2 discharge function is controlled by an external control input DISC2 (DISC½=Hi, Discharge VBUS½ to GND; DISC½=Lo. Disable VBUS½ discharge function). The internal discharge resistance is around 190Ω.

Take Power from MOUT Pin

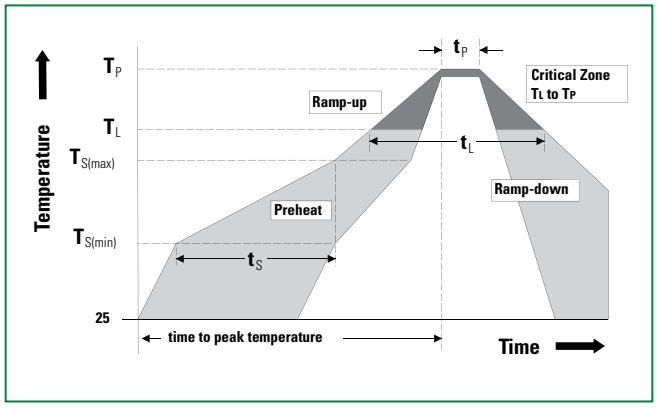
The LS24062RQ23 integrates two N-channel power switch M1 and M2 in series with a common drain output MOUT. Although MOUT pin can provide power to the other circuitry when EN1/EN2 pin is pulled high, need to pay extra attention when use it. Bypass MOUT to GND with a minimum 0.1µF MLCC capacitor if MOUT pin is used. The current drawn from MOUT pin affects current limit setting accuracy at ILIM1/ILIM2 pin. Due to body diode of the power switch M1 and M2, MOUT pin is NOT protected from over-load and short circuit fault events. Whenever the supply voltage is applied on VBUS1 or VBUS2 pin, MOUT will follow the supply voltage through either the power switch M1/M2 or M1/M2 body diode. When a short circuit occurs on the MOUT pin, the current can NOT be limited by the LS24062RQ23. If over load or short circuit protection is required for the MOUT pin, recommend to add a load switch between MOUT pin and any downstream circuits.

Soldering Parameters

Average ramp up rate (Tsmin to T_P)		1~2°C/second, 3°C/second max.
Preheat & Soak	**- Temperature Min ($T_{s(min)}$)**	150°C
	- Temperature Max ($T_{s(max)}$)	200°C
	- Time (min to max) (t_s)	60 – 120 secs
Time maintained above	**- Temperature(T_L)**	217°C
	- Time(t_L)	60~150 seconds
Peak Temperature (T_P)		See Classification Temp intable1
Time within 5°C of actual peak Temperature (t_p)		30 seconds max
Ramp-down Rate		6°C/second max
Time 25°C to peak Temperature (T_P)		8 minutes Max.

Note:

1. Tolerance for peak profile Temperature(T_p) is defined as a supplier minimum and a user maximum.
2. Tolerance for time at peak profile temperature (t_p)is defined as a supplier minimum and a user maximum.



Pb-free Process – Classification Temperatures (T_C)

Package Thickness	Volume mm³ <350	Volume mm³ 350-2000	Volume mm³ >2000
<1.6mm	260°C	260°C	260°C
1.6mm–2.5mm	260°C	250°C	245°C
>2.5mm	250°C	245°C	245°C

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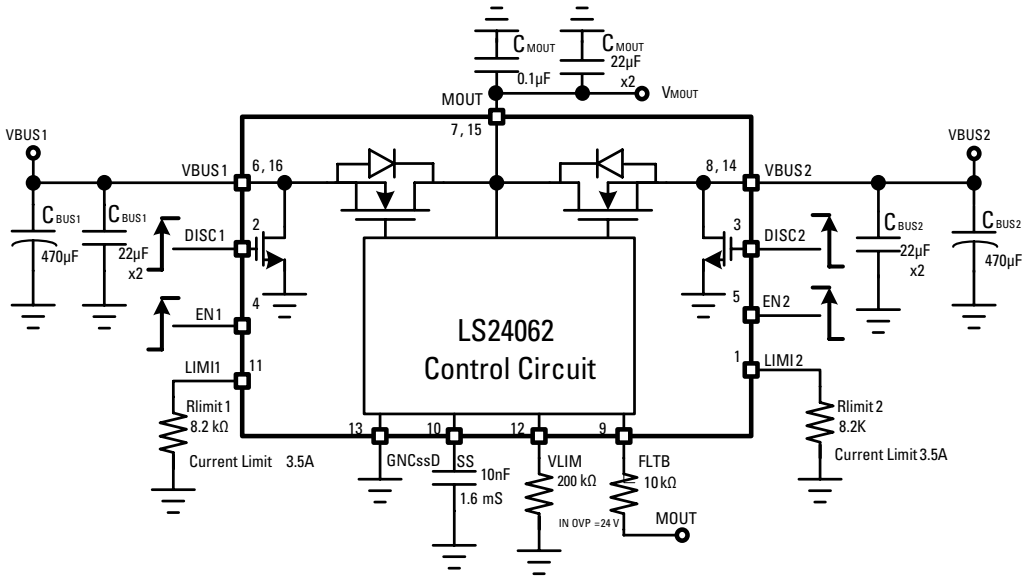
Application 1 Schematic (example)



Bill of Materials

Qty	Ref	Value	Description	Package
2	CBUS1	22 µF	Ceramic Capacitor, 50V, X5R	1206
1	CBUS1	470 µF	Electrolytic Capacitor, 50V	8x12mm
2	CMOUT	22 µF	Ceramic Capacitor, 50V, X5R	1206
1	CMOUT	0.1 µF	Ceramic Capacitor, 50V, X5R	0603
2	CBUS2	22 µF	Ceramic Capacitor, 50V, X5R	1206
1	CBUS2	470 µF	Electrolytic Capacitor, 50V	8x12mm
1	CSS	10 nF	Ceramic Capacitor, 10V, X5R	0603
2	RLIMIT1, RLIMIT2	8.2 kΩ	Resistor, ±1%	0603
1	RFLTB	10 kΩ	Resistor, ±1%	0603
1	Power IC	LS24062RQ23	eFuse	QFN2.5x3.2

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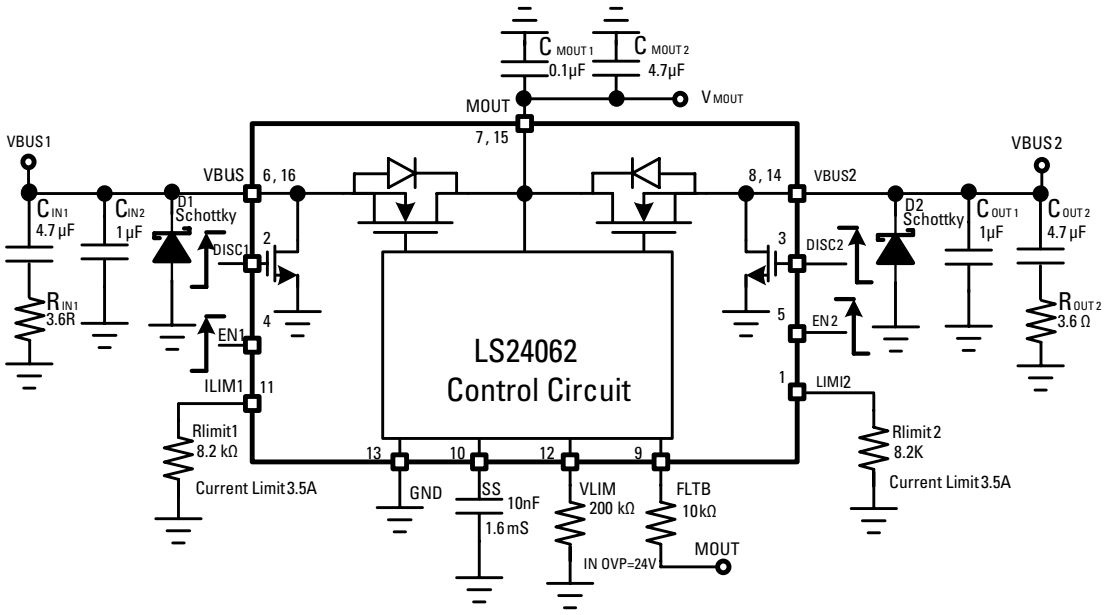
Application 2 Schematic (example) for USB Type-C Application



Bill of Materials

Qty	Ref	Value	Description	Package
2	C_{IN2} ,C_{OUT1}	1 µF	Ceramic Capacitor, 50V, X5R	805
3	C_{IN1} , C_{OUT2}, C_{MOUT2}	4.7 µF	Ceramic Capacitor, 50V, X5R	805
1	C_{MOUT1}	0.1 µF	Ceramic Capacitor, 50V, X5R	603
2	R_{IN1}, R_{OUT2}	3.6 kΩ	Resistor, ±1%	805
2	D_1 ,D_2	SL34PL	Schottky Diode	1206
1	C_{SS}	10 nF	Ceramic Capacitor, 10V, X5R	603
2	R_{LIMIT1} , R_{LIMIT2}	8.2 kΩ	Resistor, ±1%	603
1	R_{FLTB}	10 kΩ	Resistor, ±1%	603
1	R_{VLIM}	200 kΩ	Resistor, ±1%	603
1	Power IC	LS24062RQ23	eFuse	QFN2.5x3.2

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Layout Guidelines

Good PCB layout is important for improving the thermal and overall performance of LS24062RQ23. To optimize the switch response time to output short-circuit conditions, keep all traces as short as possible to reduce the effect of Power/GND trace parasitic inductance (as below red line) and add the EC capacitor (470µF) at VBUS1/VBUS2 to GND to compensate the unwanted parasitic inductance of power line (ex: USB Type C line).

- Place the input and output bypass capacitors as close as possible to the VBUS1 and VBUS2 and MOUT pins.
- IN, MOUT and OUT pins connected as below Figure 8 pattern to reduce impedance improving the power loss
- Use a ground plane to enhance the power dissipation capability of the LS24062RQ23.

Figure 15. Keep all red line traces as short as possible to reduce the effect of trace parasitic inductance.

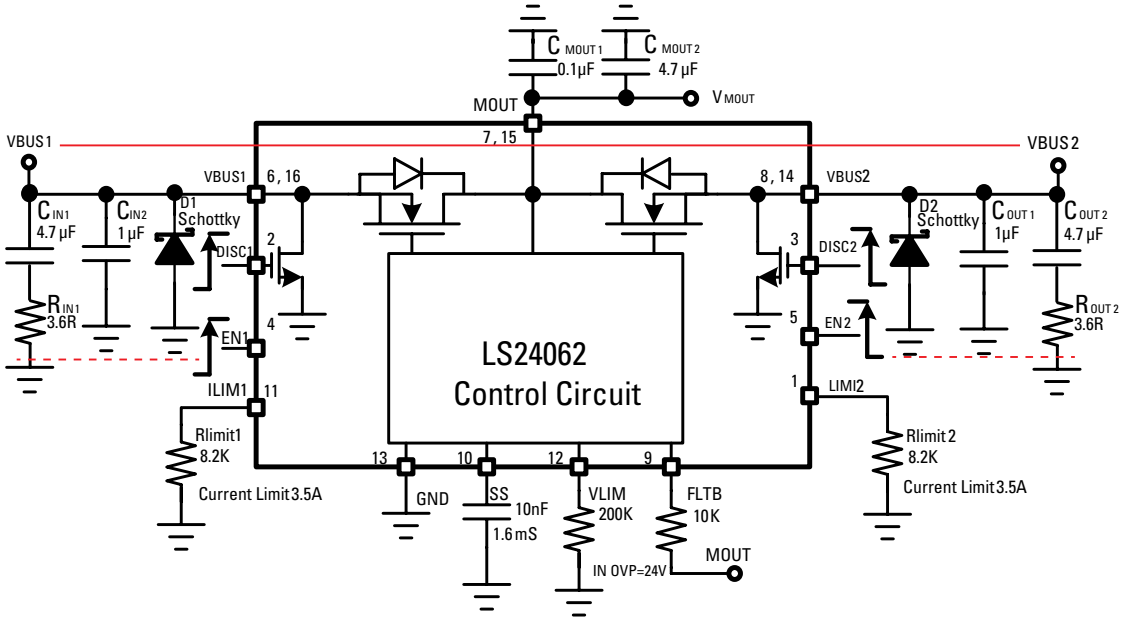
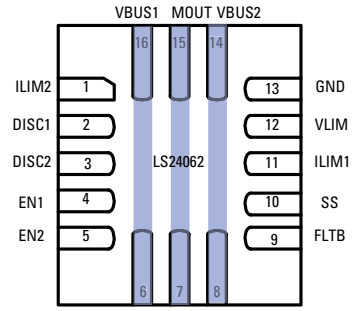
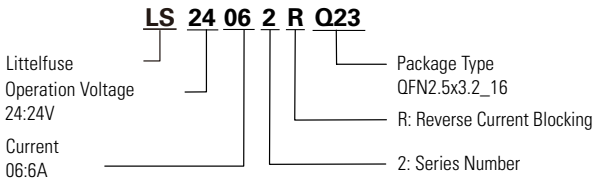


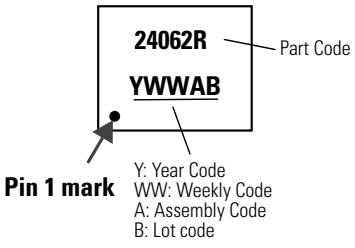
Figure 16. IN, MOUT and OUT pins connected to reduce impedance improving the power loss.



Part Numbering



Part Marking



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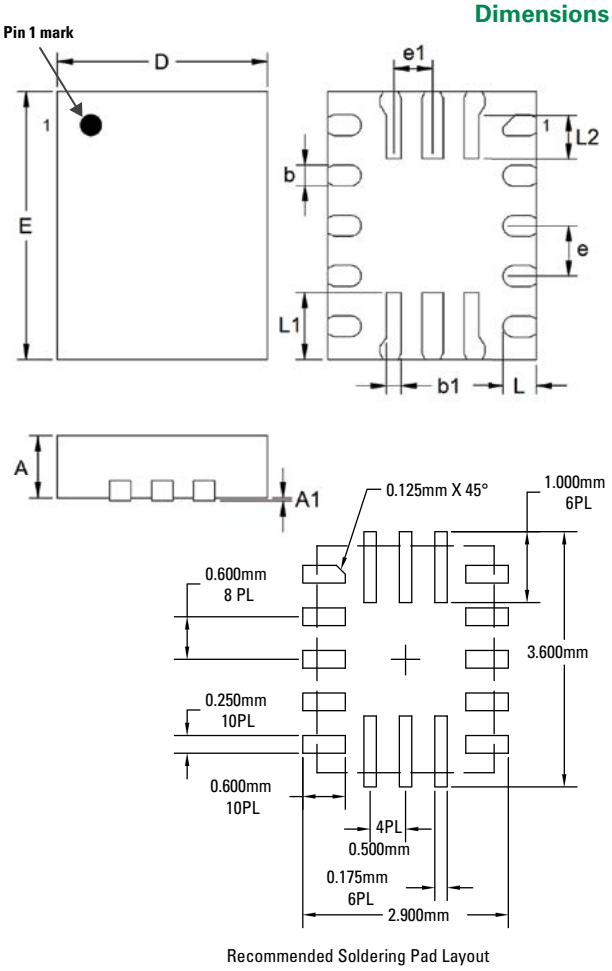
Dimensions — QFN 16L 2.5x3.2mm

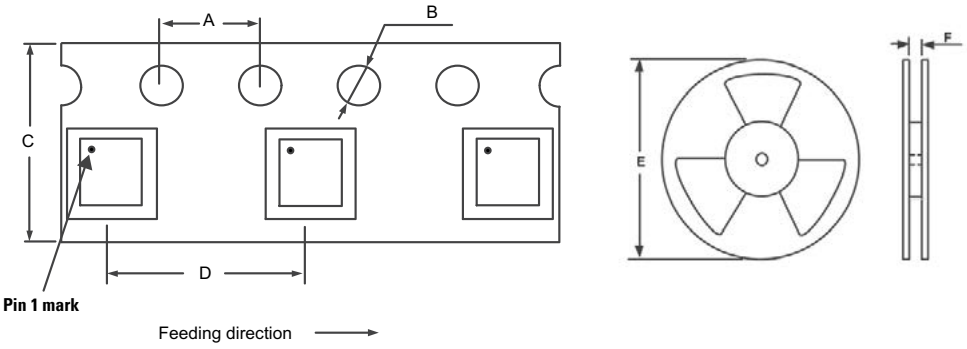


Recommended Soldering Pad Layout

Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.20	0.30	0.008	0.012
b1	0.12	0.23	0.005	0.009
D	2.40	2.60	0.094	0.102
E	3.10	3.30	0.122	0.130
e	0.60 BSC		0.024 BSC	
e1	0.50 BSC		0.020 BSC	
L	0.30	0.50	0.012	0.020
L1	0.70	0.90	0.028	0.035
L2	0.52 REF		0.020 REF	

* BSC = **B**asic **S**pacing between **C**enters

Carrier Tape & Reel Specification — QFN 16L 2.5x3.2mm



Feeding direction →

Symbol	Millimeters
A	4.0
B	1.5
C	12.0
D	8.0
E	13 inch
F	13.0

Ordering Information

Part Number	Component Package	Quantity	Packaging Option
LS24062RQ23	QFN 16L 2.5x3.2mm	5000	Tape & Reel