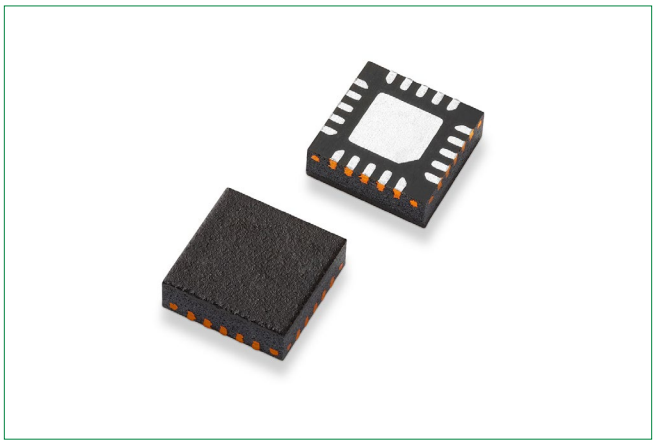
LS05006VPQ33

USB Type-C Port CC/SBU Short-to-V_{BUS} Overvoltage Protection

HF RoHS Pb



Web Resources

Download ECAD models, order samples, and find technical recources at www.littelfuse.com

Pin Description

Pin #	Pin Name	Description
SBU1I	1	Type-C connector side of SBU1 OVP FET. Connect to SBU pin of USB Type-C connector
SBU2I	2	Type-C connector side of SBU2 OVPFET. Connect to SBU pin of USB Type-C connector.
NC	3, 6, 7, 13,16,17, 19, 20	Nothing connected.
CC1I	4	Type-C connector side of CC1 OVP FET. Connect to CC pin of USB Type-C connector.
CC2I	5	Type-C connector side of CC2 OVP FET. Connect to CC pin of USB Type-C connector.
GND	8, 18, EP	Ground connection and thermal pad.
/FLT	9	Open drain fault indictor pin. Pulled down with internal FET when OVP, OTP and fault are detected.
VPWR	10	Power supply to the device and external PD controllers. Bypass VPWR to GND with a 1µF ceramic capacitor.
CC2O	11	System side of CC2 OVP FET. Connect to either CC pin of Type-C/PD controller.
CC1O	12	System side of CC1 OVP FET. Connect to either CC pin of Type-C/PD controller.
SBU2O	14	System side of SBU2 OVP FET. Connect to either SBU pin of Type-C/PD controller.
SBU1O	15	System side of SBU1 OVP FET. Connect to either SBU pin of Type-C/PD controller.

Description

The LS05006VPQ33 is a protection device that helps prevent damage to electronic products with USB Type-C ports. It protects against short circuits, overvoltage up to 24 V, and electrostatic discharge (ESD). Many USB Type-C products don't meet the Type-C specification, and some adapters that only provide 20 V to V_{BUS} can cause short circuits due to pin issues, twisting, or moisture. Proper overvoltage protection, helps avoid damage to the low -voltage silicon circuits in Type-C controllers. LS05006VPQ33, safeguards the downstream low -voltage circuits against overvoltage and IEC61000-4-2 ESD strike.

The LS05006VPQ33 has a CC pin pull-down resistor that helps power up and charge mobile devices with dead batteries. Once the system power is up, the device automatically cuts out the CC pin pull-down resistor, allowing the Type-C controller's CC pin pull-down resistor to take over without confusing the power source.

Features and Benefits

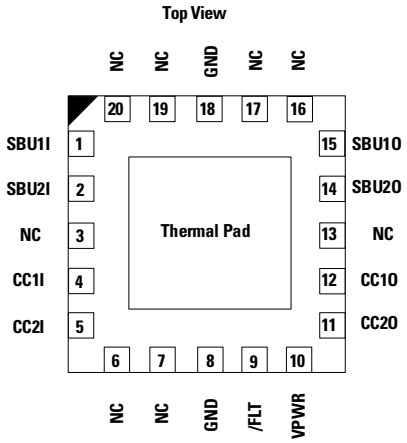
- Automatically processes signals and works transparently without interference or burdening Type-C controller operation.
- Overvoltage protection for four-channels (CCxI, SBUxI) with 24 V tolerant switch and IEC 61000-4-2 ESD protection.
- Up to 600 mA high current capability for CC1/CC2 overvoltage protection FETs to pass V_{CONN} power.
- Include integrated CC1/CC2 pull-down resistors to handle mobile device's dead battery conditions.
- Designed in a compact package QFN3x3_20L

Applications

- USB Type-C Devices
- Notebooks
- Desktops
- Monitors
- Industry PCs
- Point of Sales
- Smart Phones
- Tablets
- Docking Stations

Pinout Designation

Top View



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Absolute Maximum Rating (Reference to GND)

Symbol	Value	Units
VPWR,/FLT	-0.3 to +6	V
CC1O,CC2O,SBU1O,SBU2O	-0.3 to +6	V
CC1I,CC2I,SBU1I,SBU2I	-0.3 to +28	V
Lead Temperature (Soldering 10 s)	260	°C
Junction Temperature Range	-40 to +150	°C
Storage Temperature Range	-65 to +150	°C
ESD, Human Body Model (HBM)	±2000	V
IEC61000-4-2 Contact Discharge (CC1, CC2,SBU1, SBU2)	±8000	V

Notes: Stress exceeding those listed "Absolute Maximum Ratings" may damage the device.

Thermal Information

Symbol	Value	Units
Maximum Power Dissipation (T_A = 25 °C)	1.3	W
Thermal Resistance (θ_{JA})	96	°C/W
Thermal Resistance (θ_{JC})	44	°C/W

Notes:

1. Measured on JESD51-7, 4-Layer PCB.

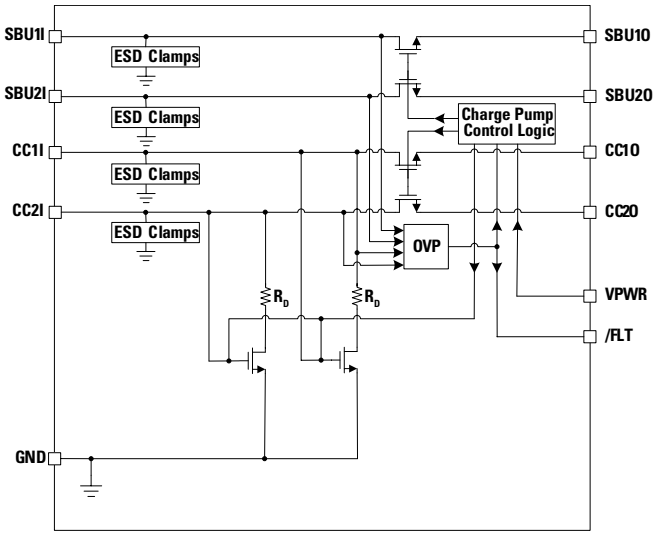
2. The maximum allowable power dissipation is a function of the maximum junction temperature T_{J_MAX}, the junction to ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_{D\_MAX} = (T_{J\_MAX}-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.

Recommend Operating Conditions

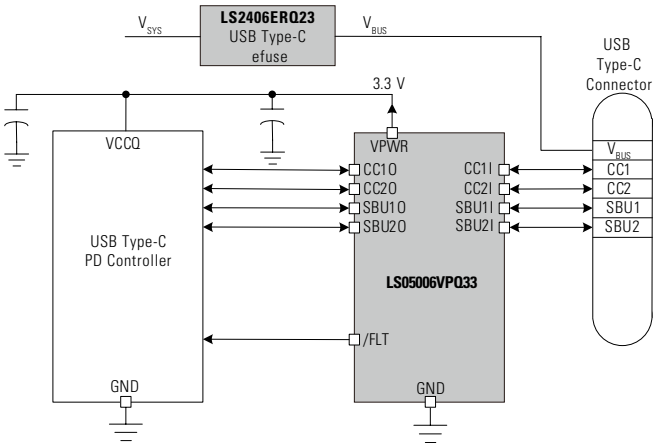
Symbol	Value	Units
CC1I, CC2I, CC1O, CC2O	0 to +5.5	V
SBU1I, SBU2I, SBU1O, SBU2O	0 to +4.3	V
Junction Temperature Range, T_J	-40 to +125	°C

Note: The device is not guaranteed to function outside of the recommended operating conditions.

Functional Block Diagram



Typical Applications



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Electrical Characteristics (T_A = +25 °C, unless otherwise specified. Typical values are at VPWR = 3.3 V.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
CC Pin OVP MOSFET						
R_{ON}		CCxO = 5V, $T_J \leq 105$ °C		250		mΩ
$R_{ON(FLAT)}$	On resistance flatness	Sweep CCxO voltage from 0 V to 1.2 V			5	mΩ
C_{ON_CC}	Equivalent on capacitance	Capacitance from CCxI or CCxO to GND when device is powered. V_{CCxI} / V_{CCxO} = 0 V to 1.2 V, f = 400 kHz		50		pF
R_D	Dead battery pull-down resistance (only present when device is unpowered). Effective resistance of R_D and FET in series	V_CCxI = 2.6 V	4.1	5.1	6.1	kΩ
V_{TH_DB}	Threshold voltage of the pulldown FET in series with R_D during dead battery	I_CCxI = 80 µA		0.76		V
V_{OVPCC}	OVP threshold on CCxI pins	Sweep CCxI pin from 5.5 V to 6.5 V until CC FETs turn off.		6.06		V
V_{OVPCC_HYS}	Hysteresis on CCxI OVP	Sweep CCxI pin from 6.5 V to 5.5 V until CC FETs turn on.		85		mV
BW_{ON}	On bandwidth single ended (-3 dB)	-3 dB bandwidth from CCxI to CCxO. Single ended measurement, 50Ω system. Vcm = 0.1 V to 1.2 V		100		MHz
$V_{ST\_VBUS\_CC}$	Short-to-V_{BUS} tolerance on the CCxI pins	Hot plug CCxI pins with a 1 meter USB Type-C Cable. Place a 30 Ω resistor on CCxO pins.			24	V
$V_{ST\_VBUS\_CC\_CLAMP}$	Short-to-V_{BUS} system-side clamping voltage on the CCxO pins	Hot-Plug CCxI with a 1 meter USB Type-C Cable. Hot-Plug voltage CCxI = 24 V. VPWR = 3.3 V. Place a 30 Ω resistor on CCxO pins.		8		V
SBU Pin OVP MOSFET						
R_{ON}		SBUxO = 3.6 V, $T_J \leq 85$ °C		4		Ω
$R_{ON(FLAT)}$	On resistance flatness	Sweep SBUxO voltage from 0 V to 3.6 V, -40 °C ≤ T_J ≤ +85 °C		0.7		Ω
C_{ON_SBU}	Equivalent on capacitance	Capacitance from SBUxI or SBUxO to GND when device is powered. V_{SBUx}I/V_{SBUxO} = 0.3 V to 3.6 V.		11		pF
V_{OVPSBU}	OVP threshold on SBUxI pins	Sweep SBUxI pin from 4 V to 5 V until SBU FETs turn off.		4.5		V
V_{OVPSBU_HYS}	Hysteresis on SBUxI OVP	Sweep SBUxI pin from 5 V to 4 V until SBU FETs turn on.		50		mV
BW_{ON}	On bandwidth single ended (-3 dB)	-3 dB bandwidth from SBUxI to SBUxO. Single ended measurement, 50 Ω system. Vcm = 0.1 V to 3.6 V		1000		MHz
X_{TALK}	Crosstalk	Measure crosstalk at f = 1 MHz from SBU1O to SBU2I or SBU2O to SBU1I. Vcm1 = 3.6 V, Vcm2 = 0.3 V. Be sure to terminate open sides to 50 Ω.		-80		dB
$V_{ST\_VBUS\_SBU}$	Short-to-V_{BUS} tolerance on the SBUxI pins	Hot plug SBUxI pins with a 1 meter USB Type-C Cable. Place a 0.1 µF capacitor in series with a 40 Ω resistor to ground on SBUxO pins.			24	V
$V_{ST\_VBUS\_SBU\_CLAMP}$	Short-to-V_{BUS} system-side clamping voltage on the SBUxO pins	Hot Plug SBUxI pins with a 1 meter USB Type-C Cable. Hot-Plug voltage SBUxI = 24 V. VPWR = 3.3 V. Place a 0.15 µF capacitor in series with a 40 Ω resistor to ground on SBUxO pins.		8		V

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Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Power Supply and Leakage Current						
I_{Q_VPWR}	VPWR quiescent current	VPWR = 3.3 V.		120		µA
I_{CC_LEAK}	Leakage current for CC pins when device is powered.	VPWR = 3.3 V, V_{CCxI} = 3.6 V, CCxO pins are floating, measure leakage into CCxI pins. Result must be same if CCxO side is biased and CCxI is left floating.		4.5		µA
I_{SBU_LEAK}	Leakage current for SBU pins when device is powered.	VPWR = 3.3 V, V_{SBUxI} = 3.6 V, SBUxO pins are floating, measure leakage into SBUxI pins. Result must be same if SBUxO side is biased and SBUxI is left floating.		0.1		µA
$I_{CCxI\_LEAK\_OVP}$	Leakage current for CC pins when device is in OVP	VPWR = 3.3 V, V_{CCxI} = 24 V, CCxO pins are set to 0 V, measure leakage into CCxI pins.		850		µA
$I_{CCxO\_LEAK\_OVP}$	Leakage current for CC pins when device is in OVP	VPWR = 0 V or 3.3 V, V_{CCxI} = 24 V, CCxO pins are set to 0 V, measure leakage out of CCxO pins.		0.1		µA
$I_{SBUxI\_LEAK\_OVP}$	Leakage current for SBU pins when device is in OVP	VPWR = 0 V or 3.3 V, V_{SBUxI} = 24 V, SBUxO pins are set to 0 V, measure leakage into SBUxI pins.		400		µA
$I_{SBUxO\_LEAK\_OVP}$	Leakage current for SBU pins when device is in OVP	VPWR = 0 V or 3.3 V, V_{SBUxI} = 24 V, SBUxO pins are set to 0 V, measure leakage into SBUxO pins.		0.1		µA
VPWR	Input supply range	External Supply Voltage	2.7		5.5	V
V_{UVLO_H}	VPWR under voltage lockout	VPWR Rising		2.40		V
V_{ULVO_HYS}	VPWR UVLO hysteresis	VPWR Falling		-0.2		V
/FLT Pin						
V_{OL}	Low level output voltage	CC pins or SBU pins are in OVP, $I_{/FLT}$ = 3 mA, measure the /FLT pin voltage.			0.4	V
$t_{OVP\_FLT\_ASSERTION}$	Time from OVP asserted to /FLT pin assertion			36		µs
$t_{OVP\_FLT\_DEASSERTION}$	Time from CC FETs turn on after an OVP to /FLT de-assertion			4		ms
Over Temperature Protection						
T_{SD_R}	Thermal shutdown	Rise temperature when /FLT is asserted.		150		˚C
T_{SD_HYS}	Thermal shutdown hysteresis	Fall temperature when /FLT is deasserted.		30		˚C

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Timing						
t_{ON_FET}	Time from VPWR rise above UVLO until CC and SBU OVP FETs are on	Sweep VPWR from 2 V to 3 V, measure time from UVLO to OVP FETs begin to turn on.		1.3		ms
$t_{ON\_FET\_DB}$	Time from crossing rising VPWR UVLO until CC and SBU OVP FETs are on and the dead battery resistors are turned off	Sweep VPWR from 2 V to 3 V, measure time from UVLO to CCxI pins dead battery resistors are disconnected.		4		ms
$d_{VPWR\_OFF/dt}$	Minimum slew rate allowed to guarantee CC and SBU FETs turn off during a power off	VPWR power off. Power off slew rate is 5 V -> 0 V in 10 µs.	-0.5			V/µs
$t_{OVP\_RESPONSE\_CC}$	OVP response time on the CC pins. Time from OVP asserted until OVP FETs turn off.	VPWR = 3.3 V		70		ns
$t_{OVP\_RESPONSE\_SBU}$	OVP response time on the SBU pins. Time from OVP asserted until OVP FETs turn off.	VPWR = 3.3 V		80		ns
$t_{OVP\_RECOVERY\_CC\_1\_FET}$	The minimum time duration until the CC FETs turn back on after OVP event. OVP must be removed for CC FETs to turn back on			0.93		ms
$t_{OVP\_RECOVERY\_CC\_1\_DB}$	The minimum time duration until the CC FETs turn back on and the dead battery resistors turn off. OVP must be removed for CC FETs to turn back on			3.6		ms
$t_{OVP\_RECOVERY\_SBU\_1}$	The minimum time duration until the SBU FETs turn back on. OVP must be removed for SBU FETs to turn back on			0.62		ms
$t_{OVP\_RECOVERY\_CC\_2\_FET}$	Time from OVP removal until CC FETs turn back on, if device has been in OVP > 0.6 ms			0.61		ms
$t_{OVP\_RECOVERY\_CC\_2\_DB}$	Time from OVP removal until CC FETs turn back on and dead battery resistors turn off, if device has been in OVP > 0.6 ms			3.3		ms
$t_{OVP\_RECOVERY\_SBU\_2}$	OVP recovery time on the SBU pins. Time from OVP removal until SBU FETs turn back on, if device has been in OVP > 0.6 ms			0.3		ms

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Detailed Description

The LS05006VPQ33 is a protection solution for USB Type-C ports. It prevents short circuits and electrostatic discharge (ESD) from damaging devices connected to the port. CC and SBU pins are near the VBUS pins in a Type-C connector, which can create a risk of short circuits. These pins must be 24 V tolerant to protect the devices, even if their operating voltage is lower. LS05006VPQ33 provides 24 V short-to-VBUS overvoltage protection for the Type-C port's CC1, CC2, SBU1, and SBU2 pins. It also offers IEC 61000-4-2 ESD protection for the CC1I, CC2I, SBU1I, and SBU2I pins.

The system has no power in a dead battery condition, and VPWR is unavailable. If LS05006VPQ33 is unpowered, the integrated CC pin pull-down resistor will activate, and the pull-up resistor will connect from a power adapter, allowing V_{BUS} voltage. When power is restored, LS05006VPQ33 conducts CC and SBU FETs to establish a handshake with the PD power source, then releases the dead battery resistor in several milliseconds to ensure the CC line pull-down resistor is 5.1 kΩ. Otherwise, the power adapter may interpret this behavior as a port disconnect and remove the V_{BUS} voltage.

Application Information

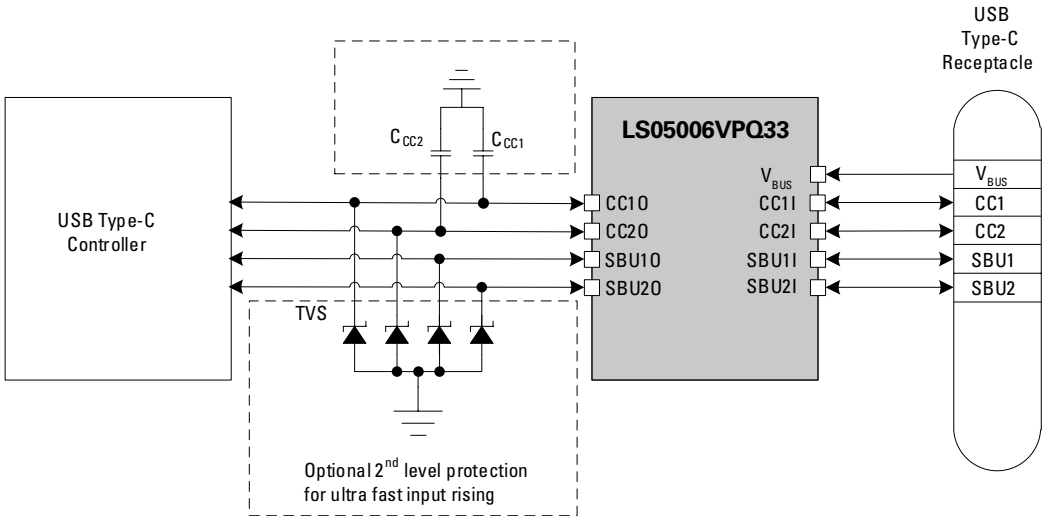
LS05006VPQ33 offers two overvoltage protection circuits - passive clamping and active protection. In case of a short circuit between CCxI/SBUxI pins and V_{BUS}, the passive clamping circuit will limit the voltage on CCxO/SBUxO pins. Then within 70 nanoseconds, the active protection circuit will turn off the switch to protect downstream low voltage devices. These circuits provide sufficient protection for downstream devices in most cases.

However, in some cases, a short circuit might occur at the Type-C connector with very low impedance, causing an ultra-fast overvoltage event on CCxI/SBUxI pin that can spike up to 10 V for a very short time. Suppose downstream devices are sensitive to this overstress. In that case, adding a second-level protection device like a transient voltage suppressor (TVS) with an appropriate trigger voltage on CCxO/SBUxO pins is recommended to limit the voltage stress on those pins even with ultra-fast input overvoltage events.

CC Line Capacitance

When USB PD is being used, the total amount of capacitance should be between 200 pF and 600 pF.

If you connect CC1O to C_{CC1} and CC2O to C_{CC2}, the total capacitance on the CC line is the sum of LS05006VPQ33 CC pin capacitance,the PD controller CC pin capacitance, and C_{CC1}/C_{CC2} capacitance. The LS05006VPQ33 CC pin capacitance is between 43 pF and 65 pF. Choose the capacitance of C_{CC1}/C_{CC2} based on your PD controller. But the total capacitance, including the CC pin and the C_{CC1}/C_{CC2} capacitance, should always be between 200 and 600 pF.



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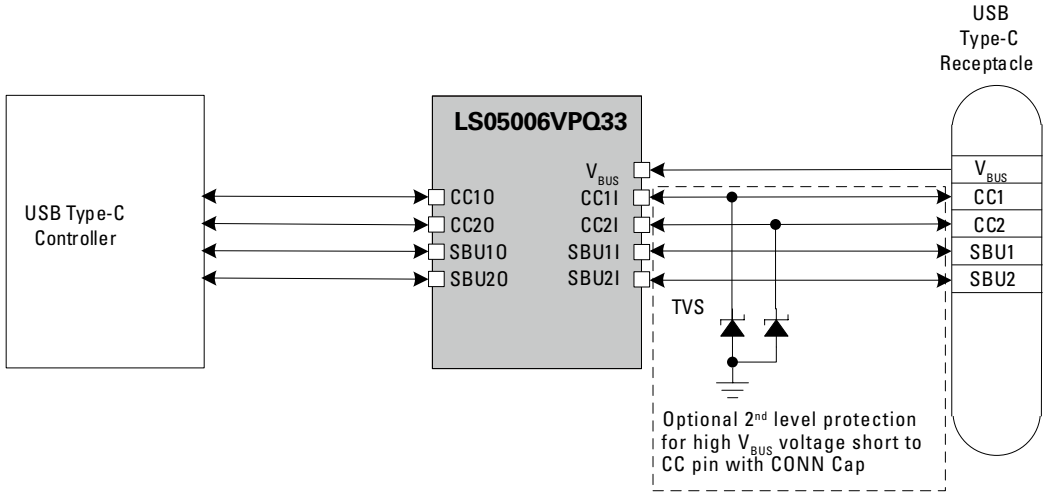
The CC channel can be used as either a signal channel or a V_{CONN} power channel for the active cable. However, if you use the CC channel as a V_{CONN} power path, there will be a high capacitance on the CCxO pin. This condition can cause a high transient current during a V_{BUS} to CC short with a long cable, especially when using a high voltage V_{BUS} like 28 V. When the internal passing switching is turned off, this high current and long cable will generate a high voltage spike on the CCxI pin with high energy. This spike could cause internal damage to LS05006VPQ33. Adding a second-level protection device to prevent damage to the internal circuit is recommended, like a transient voltage suppressor (TVS) with an appropriate trigger voltage on the CCxI pin in cases of high V_{BUS} voltage and long cable.



Four Channels of Short-to-V_{BUS} Overvoltage Protection (CC1I, CC2I,SBU1I,SBU2I): 24 V Tolerant

USB Type-C PD requires a 20 V operation voltage for the V_{BUS} pin, which can swing up to 21 V or 21.5 V during voltage changes. LS05006VPQ33 has four channels of 24 V overvoltage protection for the CC1I, CC2I, SBU1I, and SBU2I pins of the Type-C port. This protection allows for a margin above 21.5 V.

During hot-plugging, a short-to-V_{BUS} event may occur, causing ringing up to twice the settling voltage due to the cable RLC. If the capacitance on the line derates, more than 2x ringing will be seen on the USB Type-C pins during a short-to-V_{BUS} event. To clamp the ringing to approximately 30 V, LS05006VPQ33 has IEC ESD integrated. Additionally, the device integrates 30 V DC tolerant overvoltage protection FETs to handle the ringing during a short-to-V_{BUS} event. Both features ensure that LS05006VPQ33 can handle the hot plug ring during a 24 V short-to-V_{BUS} event.

If a short event occurs on the CCxI or SBUxI pin, the overvoltage FETs will quickly turn off, preventing the CCxO and SBUxO pins from seeing high voltage and effectively protecting the PD controller.

Four Channels of IEC 6000-4-2 ESD Protection (CC1I, CC2I,SBU1I,SBU2I)

The V_{BUS}, CC1, CC2, SBU1, and SBU2 from USB Type-C Port are exposed to end-users. System ESD protection is required for devices connected to them due to potential ESD events that could occur when a DC voltage is already applied to these pins. Use a 24 V DC tolerant ESD protection to protect these channels. An LS05006VPQ33 can provide just that, as it integrates four channels of IEC 61000-4-2 ESD protection for CC1I, CC2I, SBU1I, SBU2I pins in a single chip with robust protection even with a 24 V DC voltage applied on those pins.

CC1, CC2 Overvoltage Protection FETs 600 mA Capable for Passing V_{CONN} Power

The CC pins on the USB Type-C Port can provide power to active cables called V_{CONN}. V_{CONN} voltage ranges from 3 V to 5.5 V and must be able to provide 1 W power, meaning the current ability range is from 200 mA to 333 mA. LS05006VPQ33 includes low Ron overvoltage FETs for CC pins to provide the correct voltage to active cables and can handle large enough current to provide 1 W power.

If in USB PD alternate mode, more power levels are allowed on the V_{CONN} line. LS05006VPQ33 is designed to support up to 600 mA of DC current in addition to the standard 1W required by the USB Type-C specification.

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CC Dead Battery Function for Handling the Dead Battery Case

When the USB Type-C Port is the only power supply for a battery-powered device, the device must be able to charge from the USB Type-C Port, even when the battery is dead. RD pull-down resistors are needed to provide an effective V_{BUS} voltage. A USB Type-C CC/PD controller typically includes these RD pull-down resistors.

When no power is provided, LS05006VPQ33 will turn off CC and SBU overvoltage protection FETs to protect the PD controller in the dead battery condition. LS05006VPQ33 integrates high-voltage pull-down resistors on CC pins to allow reliable communication between the USB PD power source and the device. Once a correct handshake is established, the battery charging can start once the USB PD controller stablishes digital communication with the USB PD power source.

When LS05006VPQ33 is in a no-power condition, and the RP pull-up resistor is connected from a power adapter, this RP pull-up resistor activates the RD pull-down resistors inside LS05006VPQ33. When operating in a dead battery condition, CC pins RD pull-down resistors will be exposed, USB Type-C RP pull-up resistor will activate CC pins resistors first, guaranteeing a low V_{BUS} voltage. Once power is restored to the system and back to LS05006VPQ33 on its VPWR pin, CC and SBU overvoltage protection FETs will turn on in a pre-de-signed delay time. During this period, the USB Type-C Port CC pins will see the RD pull-down resistors of both LS05006VPQ33 and PD controller. The RD pull-down resistors will be disconnected after several milliseconds, avoiding system oscillation and ensuring the PD con-troller RD is fully exposed before removing the RD of LS05006VPQ33. This sequence helps ensure the USB Type-C source remains attached because a USB Type-C sink must have an RD present on CC pins at all times, according to the USB Type-C spec.

/FLT Pin Assertion

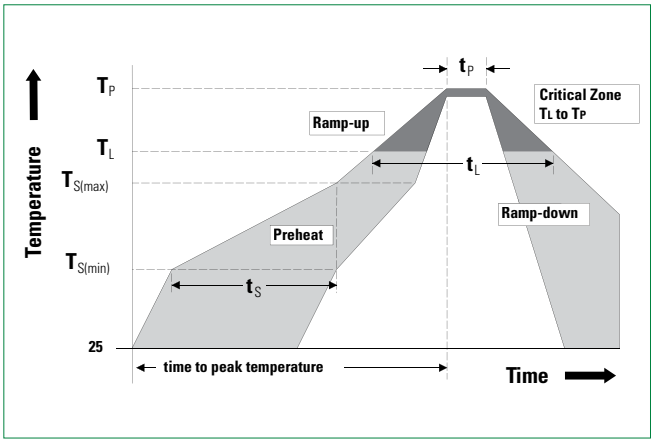
Connect a 100 kΩ resistor between the /FLT pin and VPWR pin, which is important for the LS05006VPQ33, as the /FLT pin is quickly pulled down by an internal MOSFET in just 36 µs when a fault condition like overvoltage or over temperature occurs. However, once the fault condition is resolved, there is a 4 ms blanking time before the /FLT pin pull down is released.

Soldering Parameters

Average Ramp Up Rate (Ts min to T_P)		1~2 °C/second, 3 °C/second max
Preheat & Soak	**- Temperature Min ($T_{s(min)}$)**	150 °C
	- Temperature Max ($T_{s(max)}$)	200 °C
	- Time (min to max) (t_s)	60 – 120 seconds
Time Maintained Above	**- Temperature (T_L)**	217 °C
	- Time (t_L)	60~150 seconds
Peak Temperature (T_P)		See Classification Temp Table
Time within 5 °C of Actual Peak Temperature (t_p)		30 seconds max
Ramp-down Rate		6 °C/second max
Time 25 °C to Peak Temperature (T_P)		8 minutes max

Notes:

1. Tolerance for peak profile temperature (T_p) is defined as a supplier minimum and a user maximum.
2. Tolerance for time at peak profile temperature (t_p) is defined as a supplier minimum and a user maximum.



Ordering Information

Part Number	Marking	Package	Min. Order Qty.
LS05006VPQ33	5006VP	QFN3x3_20L	5000/Tape & Reel

Pb-free Process –Classification Temperatures (TC)

Package Thickness	Volume mm^3 <350	Volume mm^3 350-2000	Volume mm^3 >2000
<1.6 mm	260 °C	260 °C	260 °C
1.6 mm–2.5 mm	260 °C	250 °C	245 °C
>2.5 mm	250 °C	245 °C	245 °C

Note: For all temperature information, please refer to topside of the package, measured on the package body surface.

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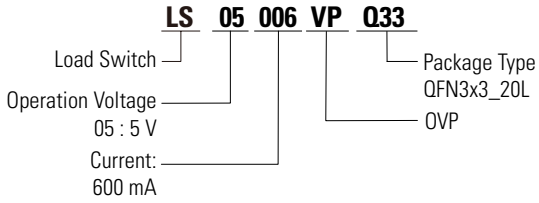
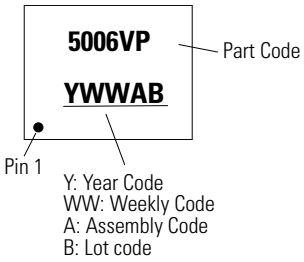
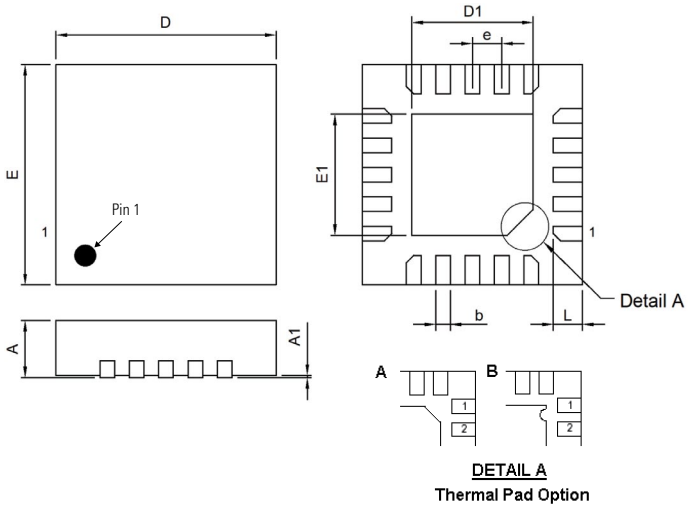
Part Numbering



Part Marking

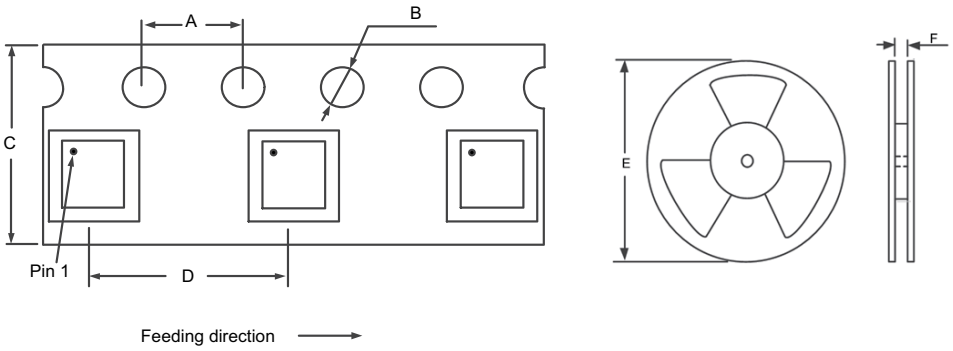


Dimensions — QFN3x3_20L



Dimension	Millimeters		Inches	
	Min	Max	Min	Max
A	0.70	0.80	0.028	0.031
A1	0.00	0.05	0.000	0.002
b	0.20	0.25	0.008	0.010
E	2.90	3.10	0.114	0.122
D	2.90	3.10	0.114	0.122
D1	1.55	1.75	0.061	0.069
E1	1.55	1.75	0.061	0.069
e	0.40		0.016	
L	0.30	0.50	0.012	0.020

Carrier Tape & Reel Specification — QFN3x3_20L



Symbol	Millimeters
A	4.0
B	1.5
C	12.0
D	8.0
E	13 inch
F	13.0

Revised: GD. 06/13/24