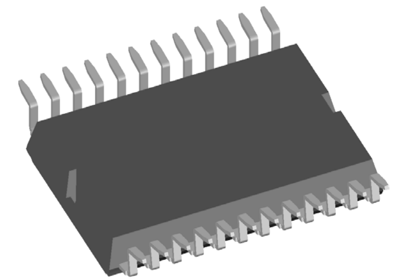
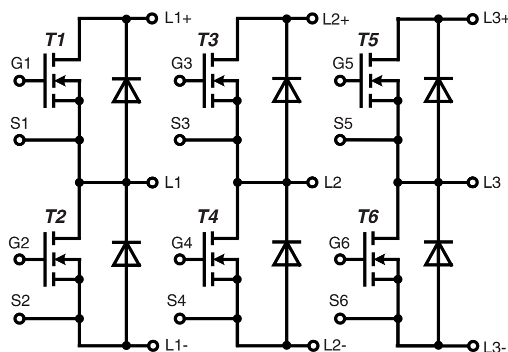
Three phase full Bridge

with Trench MOSFETs
in DCB isolated high current package

V_{DSS} = 75 V
I_{D25} = 255 A
$R_{DSon\ typ.}$ = 1.1 mΩ

Part number
MTI200WX75GD


Surface Mount Device



Features / Advantages:

- MOSFETs in trench technology:
  - low R_{DSon}
  - optimized intrinsic reverse diode
- package:
  - high level of integration
  - high current capability
  - aux. terminals for MOSFET gate control
  - terminals for soldering or welding connections
  - isolated DCB ceramic base plate with optimized heat transfer
- Space and weight savings
- High current capability

Applications:

AC drives
- in automobiles
  - electric power steering
  - starter generator
- in industrial vehicles
  - propulsion drives
  - fork lift drives
- Battery supplied equipment
- DC-DC converter

Package: ISOPLUS-DIL®

- High level of integration
- RoHS compliant
- Terminals for soldering or welding connections
- Space and weight savings
- High reliability
- Low thermal impedance

Terms & Conditions of usage
The data contained in this product data sheet is exclusively intended for technically trained staff. The user will have to evaluate the suitability of the product for the intended application and the completeness of the product data with respect to his application. The specifications of our components may not be considered as an assurance of component characteristics. The information in the valid application- and assembly notes must be considered. Should you require product information in excess of the data given in this product data sheet or which concerns the specific application of your product, please contact your local sales office.
Due to technical requirements our product may contain dangerous substances. For information on the types in question please contact your local sales office.
Should you intend to use the product in aviation, in health or life endangering or life support applications, please notify. For any such application we urgently recommend
- to perform joint risk and quality assessments;
- the conclusion of quality agreements;
- to establish joint measures of an ongoing product survey, and that we may make delivery dependent on the realization of any such measures.

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MOSFETs				Ratings		
Symbol	Definitions	Conditions	min.	typ.	max.	Unit
V_{DSS}	*drain source breakdown voltage*	T_{VJ} = 25°C to 150°C			75	V
V_{GS} V_{GSM}	*max. DC gate source voltage* *max. transient gate source voltage*				±15 ±20	V V
I_{D25} I_{D90}	*continuous drain current* *(die capability)*	T_C = 25°C T_C = 90°C			255 190	A A
$R_{DS(on)}$ [1]	*static drain source on resistance*	on chip level at T_{VJ} = 25°C I_D = 100 A; V_{GS} = 10 V T_{VJ} = 125°C		1.1 1.8	1.3	mΩ mΩ
$V_{GS(th)}$	*gate threshold voltage*	I_D = 275 µA; V_{DS} = V_{GS} T_{VJ} = 25°C	2.3	3.1	3.8	V
I_{DSS}	*drain source leakage current*	V_{DS} = V_{DSS}; V_{GS} = 0 V T_{VJ} = 25°C T_{VJ} = 125°C		 10	1 100	µA µA
I_{GSS}	*gate source leakage current*	V_{GS} = ±20 V; V_{DS} = 0 V			500	nA
R_G	*gate resistance*	on chip		2.7		Ω
C_{iss} C_{oss} C_{rss}	*input capacitance* *output capacitance* *reverse transfer capacitance*	V_{GS} = 0 V; V_{DS} = 38 V; f = 1 Mhz		10.8 2.42 110	14.4 3.22 -	nF nF pF
Q_g Q_{gs} Q_{gd}	*total gate charge* *gate source charge* *gate drain (Miller) charge*	V_{GS} = 10 V; V_{DS} = 38 V; I_D = 100 A		155 53 32		nC nC nC
$t_{d(on)}$ t_r $t_{d(off)}$ t_f E_{on} E_{off} $E_{rec(off)}$	*turn-on delay time* *current rise time* *turn-off delay time* *current fall time* *turn-on energy per pulse* *turn-off energy per pulse* *turn-off reverse recovery losses*	inductive load T_{VJ} = 125°C V_{GS} = 10 V; V_{DS} = 30 V I_D = 100 A; R_G = 27 Ω		145 70 520 55 80 350 8		ns ns ns ns µJ µJ µJ
R_{thJC}	*thermal resistance junction to case*				0.85	K/W
R_{thJH}	*thermal resistance junction to heatsink*	with heat transfer paste (IXYS test setup)		1.1	1.4	K/W
		[1] $V_{DS} = I_D \cdot (R_{DS(on)} + 2 \cdot R_{Pin\ to\ Chip})$				

Source-Drain Diode						
I_{F25} I_{F90}	*forward current (body diode)*	V_{GS} = 0 V T_C = 25°C T_C = 90°C			175 100	A A
V_{SD}	*source drain voltage*	I_F = 100 A; V_{GS} = 0 V T_{VJ} = 25°C		0.9	1.2	V
Q_{RM} I_{RM} t_{rr}	*reverse recovery charge* *max. reverse recovery current* *reverse recovery time*	V_R = 30 V; I_F = 100 A T_{VJ} = 125°C R_G = 27 Ω		730 27 42		nC A ns

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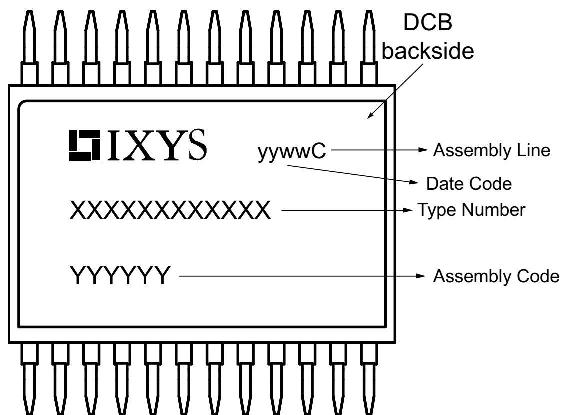
Package ISOPLUS-DIL®				Ratings			
Symbol	**Definitions**	**Conditions**		**min.**	**typ.**	**max.**	**Unit**
I_{RMS}	*RMS current*	per pin in main current paths (L1+...L3+, L1-...L3-, L1...L3) may be additionally limited by external connections (PCB tracks) 2 pins for output L1, L2, L3				75	A
T_{stg}	*storage temperature*			-55		125	°C
T_{op}	*operation temperature*			-55		150	°C
T_{VJ}	*virtual junction temperature*			-55		175	°C
Weight					13		g
F_C	*mounting force with clip*			50		250	N
V_{ISOL}	*isolation voltage*	t = 1 second	50/60 Hz, RMS, $I_{ISOL} \leq 1$ mA	1200			V
		t = 1 minute		1000			V
$R_{pin\text{-}chip}$	*resistance terminal to chip*	$V_{DS} = I_D \cdot (R_{DS(on)} + 2 \cdot R_{pin\ to\ chip})$			0.5		mΩ
C_P	*coupling capacity*	between shorted pins and back side metallization			160		pF



Part number

M = MOSFET
T = Trench
I = Infineon Trench
200 = Current Rating [A]
WX = 6-Pack with separated phase legs
75 = Reverse Voltage [V]
GD = ISOPLUS-DIL

Ordering	Part Name	Marking on Product	Delivering Mode	Base Qty	Ordering Code
Standard	MTI200WX75GD-SMD	MTI200WX75GD	Tube	13	516955

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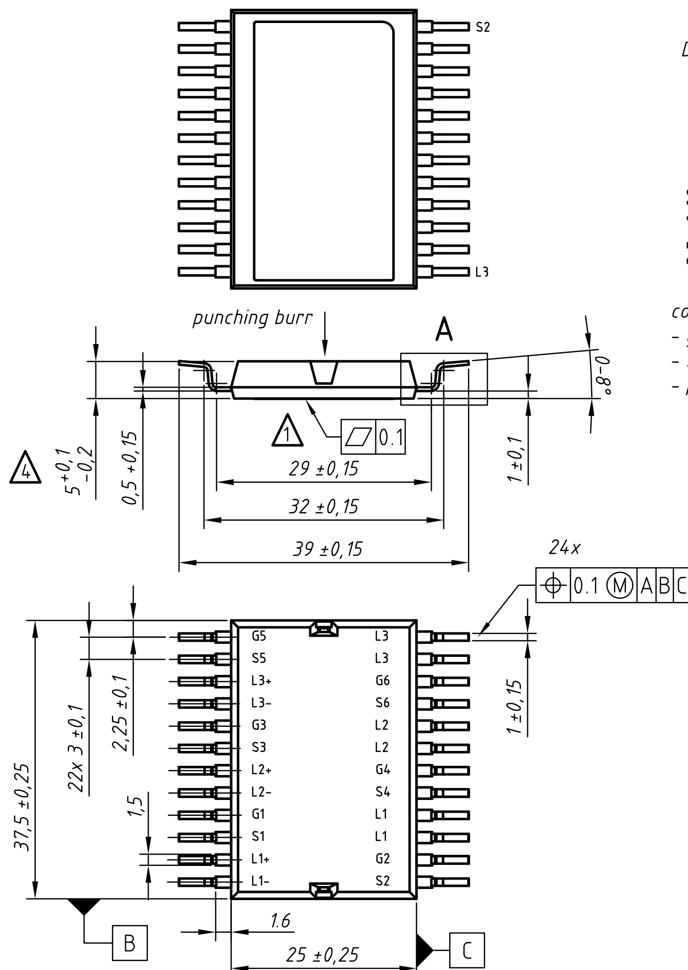
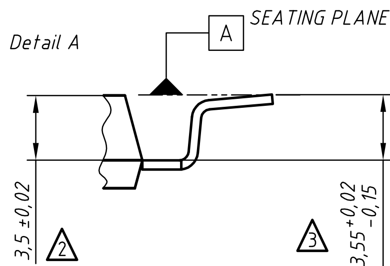
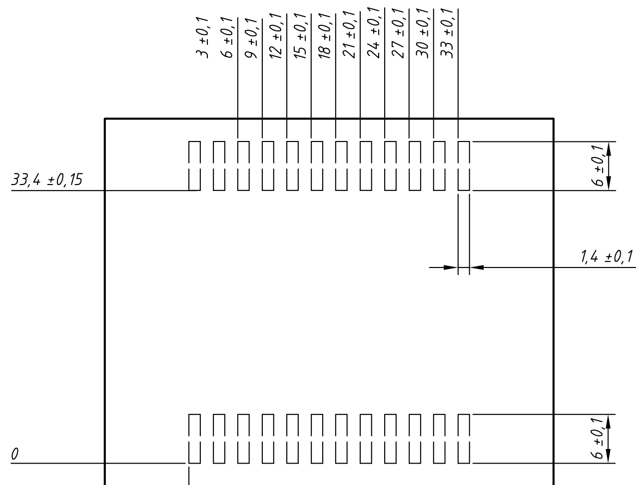
Outlines ISOPLUS-DIL®





contact pin:
- galv. tin plating, per pin side: Sn 10...25 µm, undercoating Ni 0,2...1 µm
- stamping edges may be free of tin
- puching burr: ≤ 0,05mm

1. Convex bow of substrate, typ. 10-40 µm longitudinal and 5-15 µm transversal
2. Distance between pin and case bottom side.
3. Distance between pin and contact surface.
4. Distance between parallel planes aligned to top and bottom sides of the package



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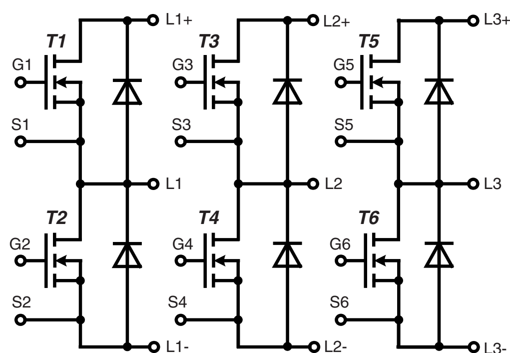
Remarks:

1) pin layout / dimensions are conditionally
2) soldering paste thickness: 200µm



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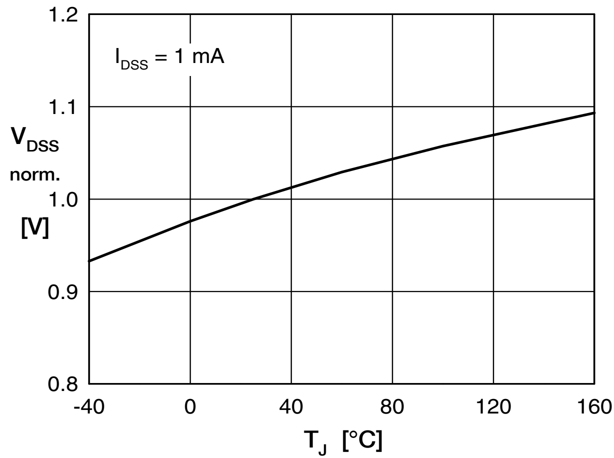

Fig.1 Drain source breakdown voltage V_{DSS} vs. junction temperature T_{VJ}

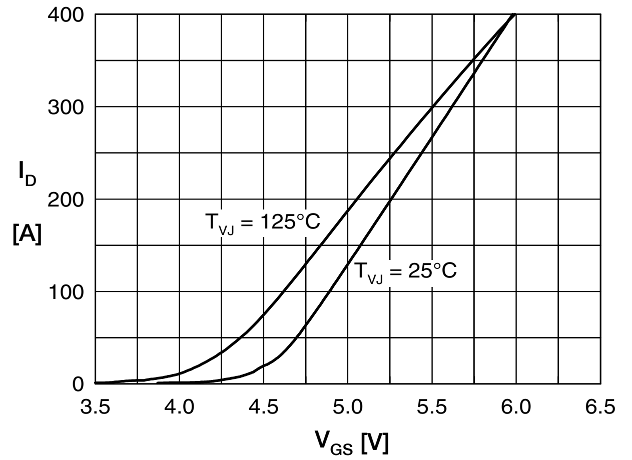

Fig. 2 Typ. transfer characteristics

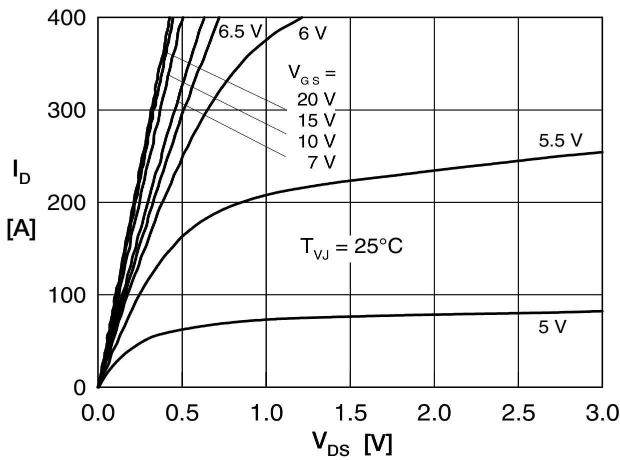

Fig. 3 Typ. output characteristics on die level

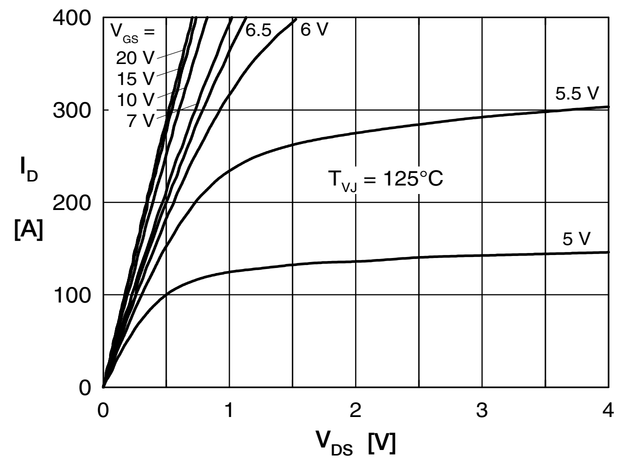

Fig. 4 Typ. output characteristics on die level

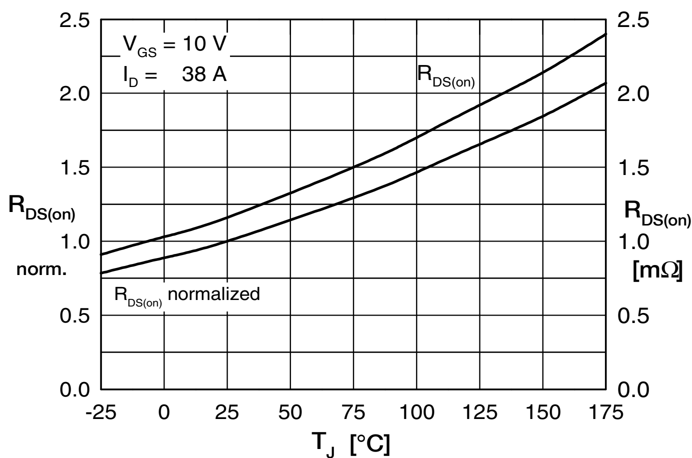

Fig.5 Drain source on-state resistance $R_{DS(on)}$ vs. junction temperature T_{VJ}, on die level

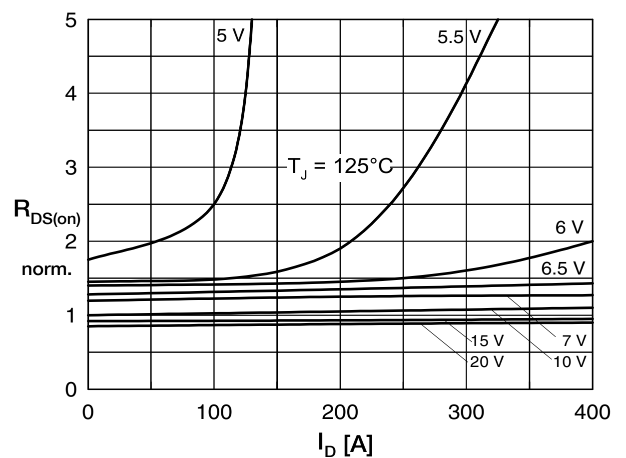

Fig. 6 Drain source on-state resistance $R_{DS(on)}$ versus I_D, on die level

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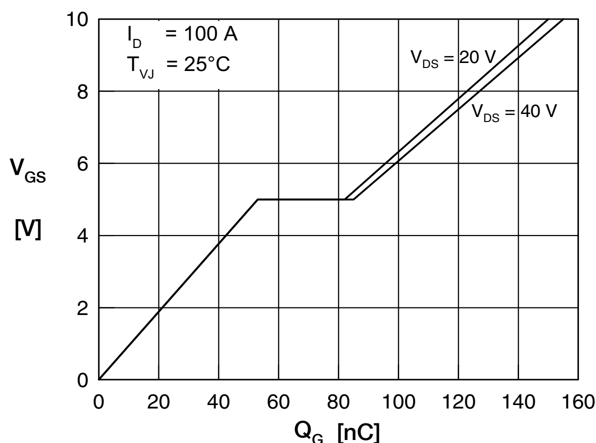

Fig.7 Typical turn on gate charge

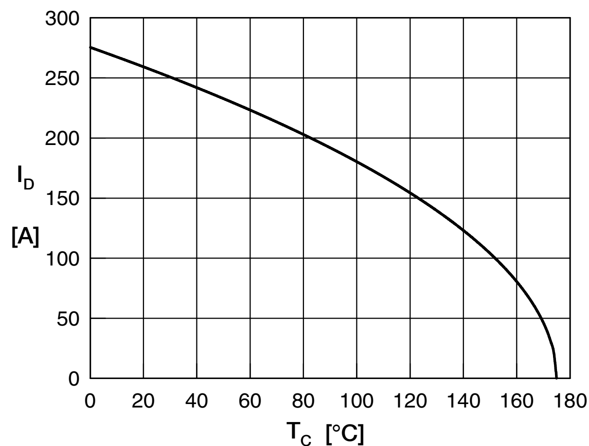

Fig. 8 Drain current I_D vs. case temperature T_C (Chip capability)

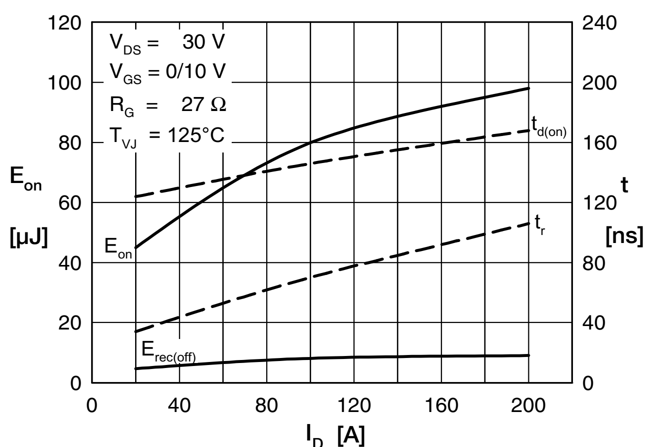

Fig. 9 Typ. turn-on energy and switching times versus drain current, inductive switching

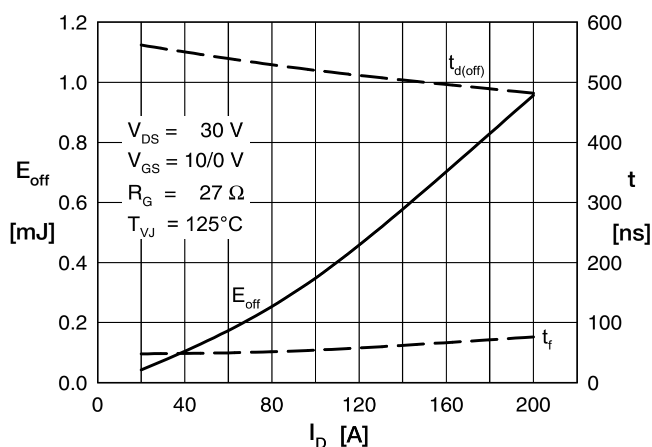

Fig. 10 Typ. turn-off energy and switching times versus drain-current, inductive switching

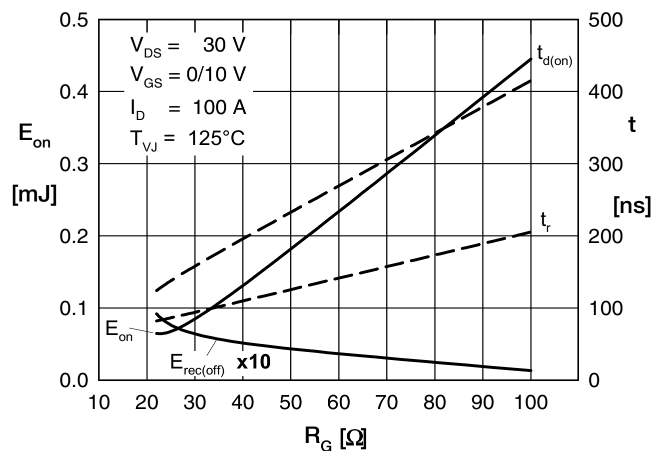

Fig. 11 Typ. turn-on energy and switching times versus gate resistor, inductive switching

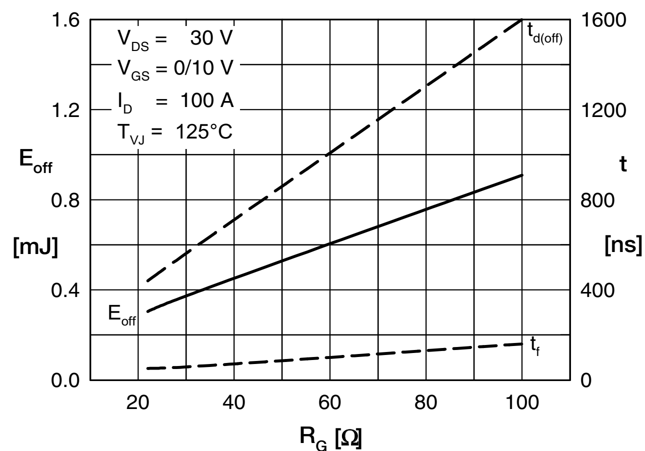

Fig. 12 Typ. turn-off energy and switching times versus gate resistor, inductive switching

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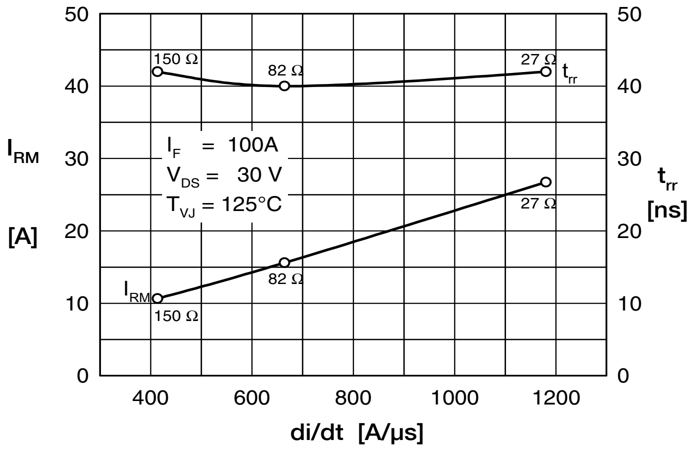

Fig. 13 Typ. reverse recovery characteristics

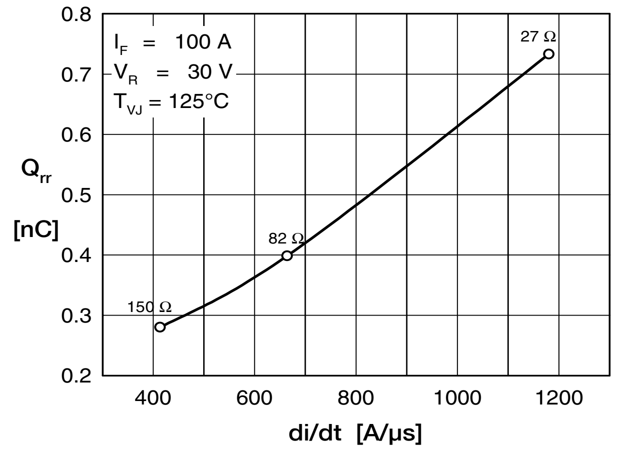

Fig. 14 Typ. reverse recovery characteristics

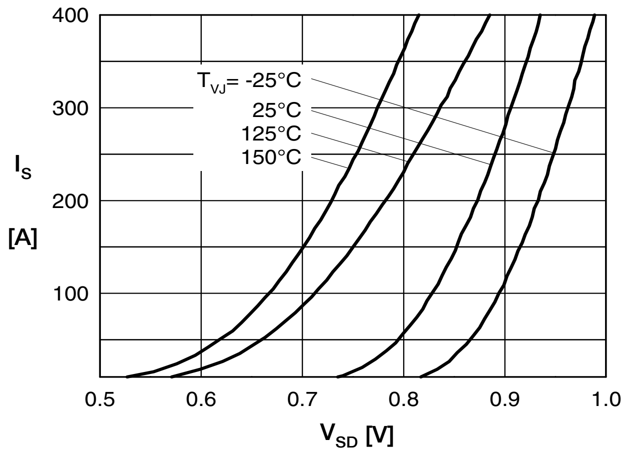

Fig.15 Source current I_S vs. source drain voltage V_{SD} (body diode) on die level

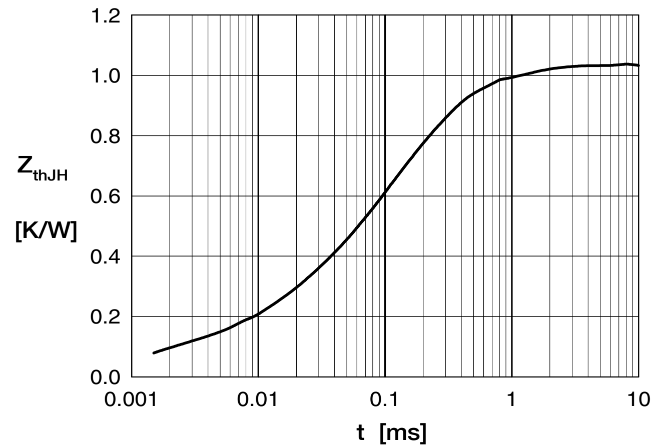

Fig. 16 Typ. thermal impedance junction to heatsink Z_{thJH} with heat transfer paste (IXYS test setup)

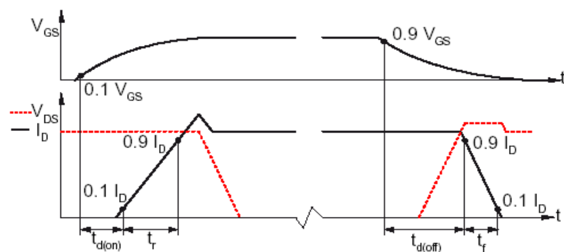

Fig. 17 Definition of switching times

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