AND8232/D

PCB Design Guidelines that Maximize the Performance of TVS Diodes

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APPLICATION NOTE

Introduction

Transient Voltage Suppressors (TVS) avalanche diodes and diode arrays can be used to protect sensitive electronic components from the surge pulses that arise from ESD and EMI. The small size, fast response time, low clamping voltage and low cost of TVS diodes provides for an effective solution to prevent surge problems. Avalanche TVS diodes and diode arrays are relatively simple devices to use to suppress surge voltages. Only a few PCB design rules must be followed to optimize the ESD and EMI immunity level of the protection circuits.

Protection Philosophy

Designing in EMI and ESD protection at the beginning of the project saves time and money, as shown in Figure 1. This is a simple concept, but often surge problems are not discovered and addressed until failures occur in the certification tests or field. Adding TVS protection to the PCB can reduce the time and money that results from adding shields and modifying cables. TVS devices can serve as a low cost preventive tool to reduce the need for expensive system modifications that often are required when EMI problems occur late in the product development cycle.

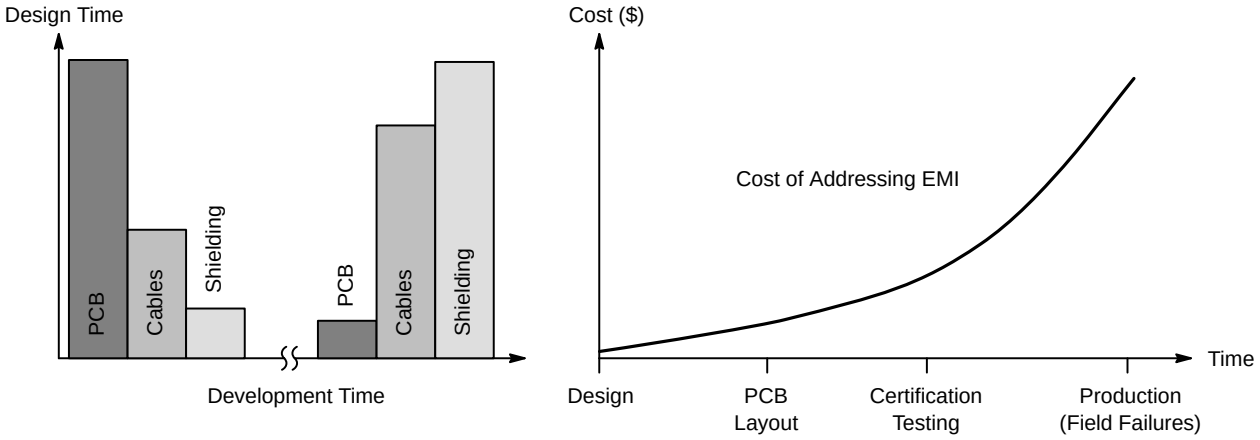

Figure 1. Addressing Potential EMI Problems at the Beginning of a Design Saves both Time and Money

PCB Layout Guidelines

The PCB layout is an important factor in creating an effective surge suppression circuit. The following PCB guidelines are recommended to enhance the performance of a TVS device:

- Locate the TVS Devices Close to the I/O Connector
- Connect the Surge Protection Circuits to Chassis or Power Ground
- Minimize the PCB's Parasitic Inductances
- Reduce the Loop Area Formed by the PCB Traces
- Select Surface Mount TVS Devices

Location

The location of the protection devices on the PCB is the simplest and most important design rule to follow. The TVS devices should be located as close as possible to the noise source. In most systems, surge pulses occur on data and power lines that enter the PCB through the I/O connector. Figure 2 provides an example of the recommended layout that places the TVS devices next to the connector.

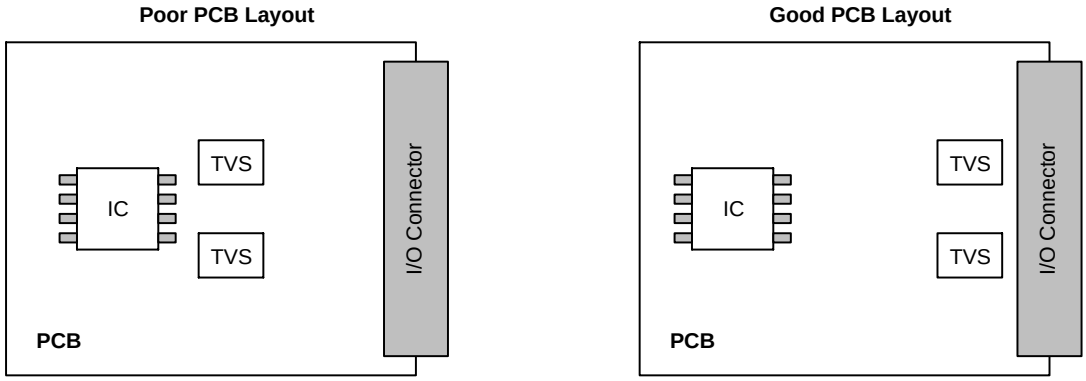

Figure 2. Locating the TVS Devices Close to the I/O Connector Ensures that a Surge Voltage Entering the PCB will be Clamped before the Pulse can be Coupled into Adjacent Traces

The length of the traces connecting the TVS devices, IC and I/O connector is a key factor that determines whether the surge currents are dissipated by the TVS devices or the IC's internal ESD protection circuit. If the TVS diodes and internal IC protection circuit have a similar turn-on voltage, the only difference between the devices will be the impedance of their PCB traces. A surge current will always follow the lowest impedance path; thus, the TVS should have a shorter trace than the IC, as shown in Figure 3. A shorter trace length equates to smaller impedance, which helps ensure that the surge energy will be dissipated by the TVS device instead of the IC.

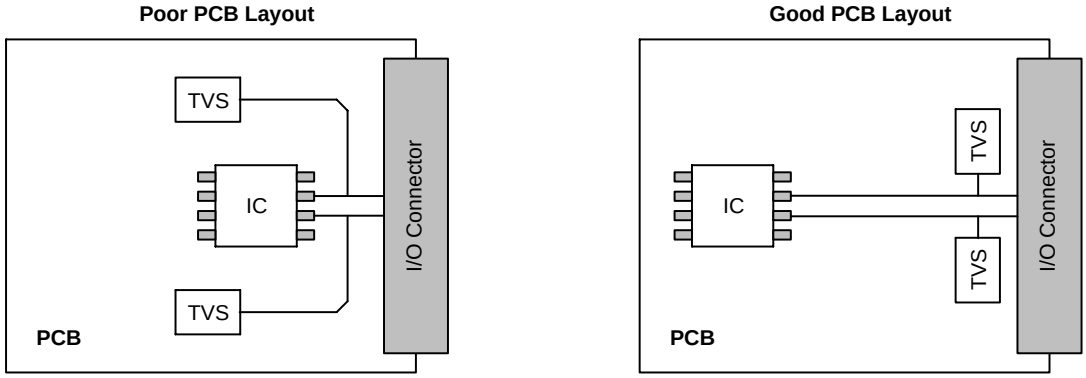

Figure 3. The Length of the Trace Connecting the TVS Device to the I/O Connector should be Minimized and Small in Comparison with the Trace between the Connector and IC

EMI protection can also be provided by locating sensitive traces in the center of the PCB rather than near the edges. Traces located near the edge of the PCB are more vulnerable to surges such as ESD, which can occur during handling. For example, the clock and reset traces on a microprocessor board can be located in the center of the PCB to provide additional protection, as shown in Figure 4.

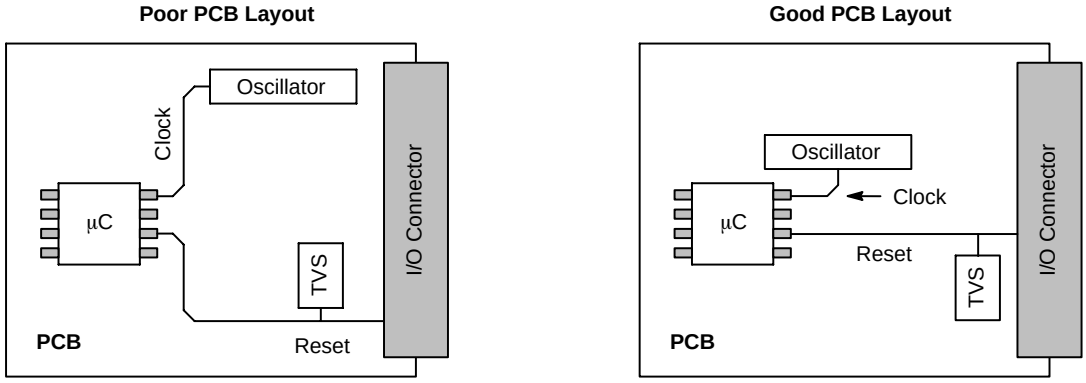

Figure 4. A Good PCB Layout Avoids Locating Critical Signal Lines Near the Edge of the PCB

Ground Selection

If possible, the protection circuits should shunt the surge voltage to either the reference or chassis ground, as shown in Figure 5. Shunting the surge voltage directly to the transceiver's signal ground can cause ground bounce. The clamping performance of TVS diodes on PCBs that use only a single ground can be improved by minimizing their ground connection impedance with a "stub" trace that is relatively short and wide.

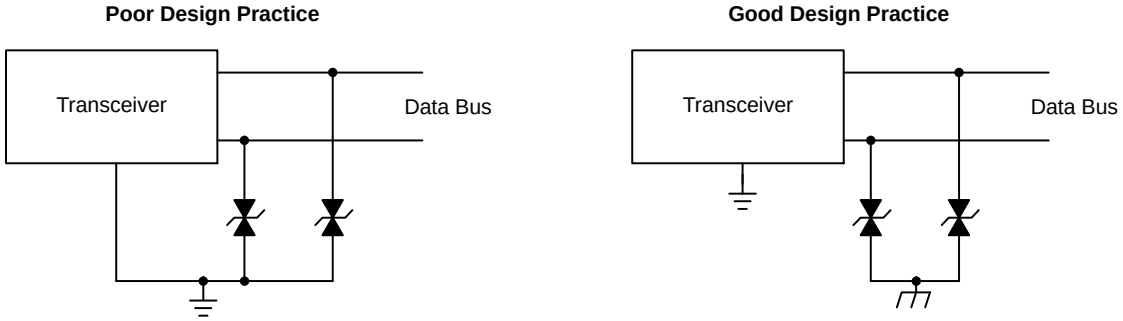

Figure 5. Connecting the TVS Devices to Either Chassis or Power Ground Helps to Prevent the Noise Signal from being Coupled into the Protected IC's Signal Ground

Parasitic Inductances

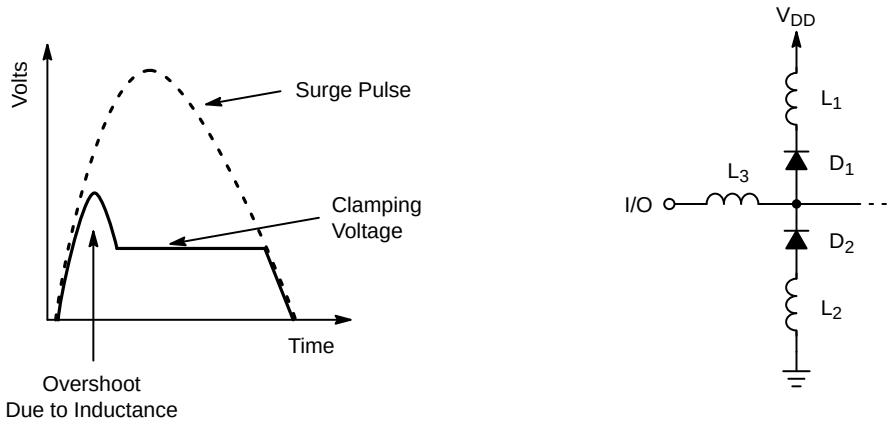

Figure 6. The PCB Layout and IC Package Parasitic Inductances Create a Short Duration Voltage Spike that Increases the Clamping Voltage of a TVS Device

The parasitic inductances produced by the PCB traces and IC package can cause a significant overshoot to the TVS's clamping voltage, as shown in Figure 6. The inductance of the PCB can be reduced by using short trace lengths and multi-layer boards with separate ground and power planes. The inductance contributed by the package is minimized by selecting small surface mount packages. Listed below are the clamping equations for a diode array that include the inductance terms.

$$\text{if } L_1 = L_2 = L_3 = 0$$

$$V_{Peak\_Positive\_Surge} = V_{DD} + V_{F\_D1}$$

$$V_{Peak\_Negative\_Surge} = -V_{F\_D2}$$

$$\text{if } L_1, L_2, \text{ and } L_3 \neq 0$$

$$V_{Peak\_Positive\_Surge} = V_{DD} + V_{F\_D1} + \left(L_1 \times \frac{dI_{Surge}}{dt}\right) + \left(L_3 \times \frac{dI_{Surge}}{dt}\right)$$

$$V_{Peak\_Negative\_Surge} = -\left[V_{F\_D2} + \left(L_2 \times \frac{dI_{Surge}}{dt}\right) + \left(L_3 \times \frac{dI_{Surge}}{dt}\right)\right]$$

September 19, 2016 − Rev. 1

Loop Area

Radiated emissions and RF susceptibility can be reduced by minimizing the loop area formed by high speed data and ground lines. One effective method to minimize loop problems is to incorporate a ground plane in the PCB design, especially when the traces are relatively long. Maximizing the separation distance from the TVS device and IC provides isolation; however, this may increase the loop area, as shown in Figure 7.

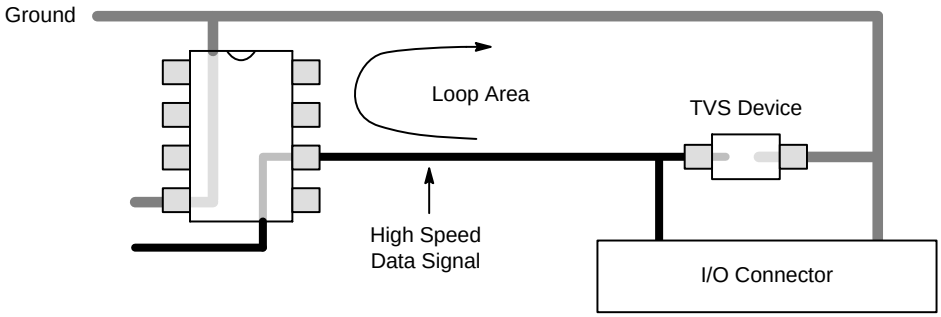

Figure 7. The Data and Ground Traces can Form a Loop that Functions as an Unintended Antenna and Increases the RF Susceptibility and Emissions of the PCB

Package Selection

The small size of a surface mount IC is an advantage for surge suppression and EMI filter devices. Inductance increases the clamping voltage of a TVS device and degrades the high frequency characteristics of an EMI filter. The inductance of a TVS diode is proportional to the size of the IC; thus, a small surface mount package typically has better EMI characteristics than a large leaded package, as shown in Figure 8.

Surge Suppression and EMI Characteristics

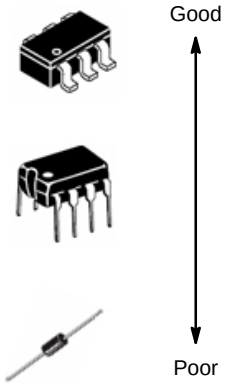

Figure 8. Surface Mount TVS Devices have Better Surge Suppression and High Frequency Characteristics than Leaded Packages

References

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[4] Lepkowski, J., “AND8231 − Circuit Configuration Options for Transient Voltage Suppression Diodes”, 2005.

[5] Lepkowski, J., “AND8230 − Application Hints for Transient Voltage Suppression Diode Circuits”, 2005.