LF2110B / LF2113B

High-Side / Low-Side Gate Driver

Expertise Applied | Answers Delivered

Features

- Drives two N-channel MOSFETs or IGBTs in high-side / low side configuration
- High-side operation up to 600V
- 2.5A source and sink typical output currents
- Outputs tolerant to negative transients
- Wide gate driver supply voltage range: 10V to 20V
- Wide logic input supply voltage range: 3.3V to 20V
- Wide logic supply offset voltage range: -5V to 5V
- 15 ns (typical) rise / 13 ns (typical) fall times with 1000 pF load
- 105 ns (typical) turn-on / 94 ns (typical) turn-off delay times
- Cycle-by-cycle edge-triggered shutdown circuitry
- Under Voltage Lockout (UVLO) for high and low side drivers
- Extended temperature range: -40 °C to +125 °C

Applications

- DC-DC Converters
- AC-DC Inverters
- Motor Controls
- Class D Power Amplifiers

Description

The LF2110B and LF2113B are high voltage, high-speed MOSFET and IGBT drivers with independent high-side and low-side outputs. An integrated floating supply enables the high-side driver to operate up to 500V for the LF2110B and up to 600V for the LF2113B. Matched maximum propagation delays of 10ns for the LF2110B and 20ns for the LF2113B allows high frequency operation.

Logic inputs for both LF2110B and LF2113B are compatible with standard CMOS levels (as low as 3.3V) while the driver outputs feature high pulse current buffers designed to minimize driver cross-conduction.

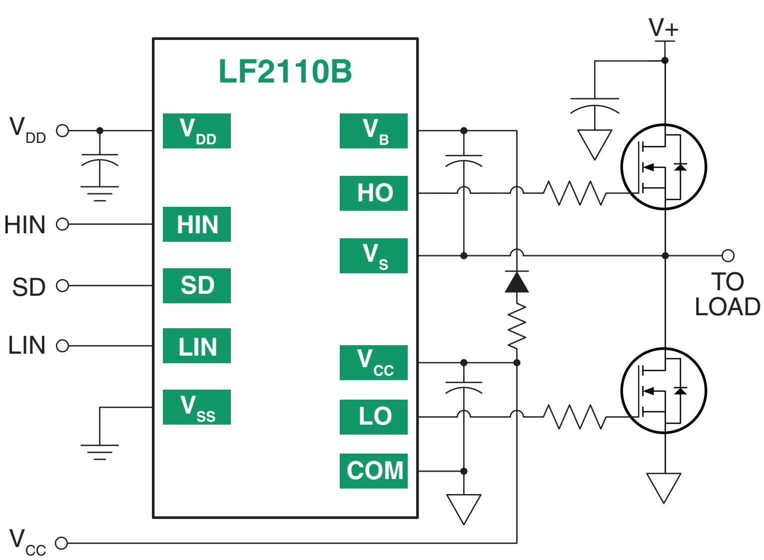
Offered in a 16-lead SOIC package, the LF2110B and LF2113B operate over an extended temperature range of -40 °C to +125 °C.

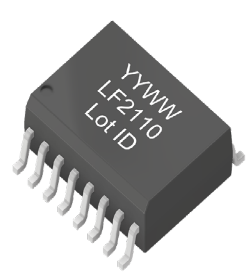
Ordering Information

YearYear WeekWeek

Part #	Package	Pack / Qty	Mark
LF2110BTR	SOIC-16	T & R / 1500	YYWW LF2110B LOT ID
LF2113BTR	SOIC-16	T & R / 1500	YYWW LF2113B LOT ID

Typical Application

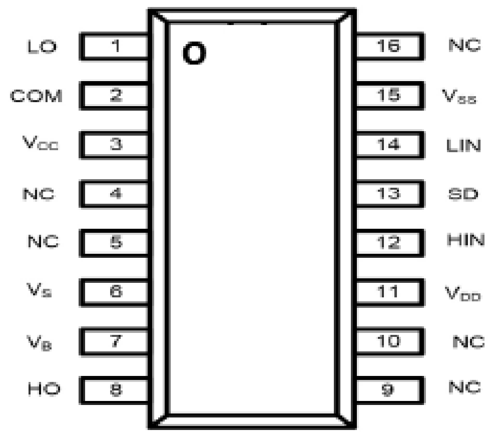




SOIC-16

1 Specifications

1.1 Pin Diagrams



Top View: SOIC-16

LF2110B / LF2113B

1.2 Pin Descriptions

Pin#	Name	Type	Description
11	V_{DD}	Power	Logic positive voltage supply
12	HIN	Input	Logic control for the high-side gate driver output. Non-Inverting
13	SD	Input	Logic control for shutdown
14	LIN	Input	Logic control for the low side gate driver output. Non-Inverting
15	V_{SS}	Power	Logic ground
7	V_B	Power	High-side gate driver floating positive voltage supply
8	HO	Output	High-side gate driver output
6	V_S	Power	High-side gate driver floating power supply return
3	V_{cc}	Power	Low-side gate driver positive voltage supply
1	LO	Output	Low-side gate driver output
2	COM	Power	Low-side gate driver power supply return
4, 5, 9, 10, 16	NC	No Connect	Not Connected Internally

1.3 Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Units
High side floating supply voltage (LF2110B)	V_B	-0.3	+524	V
High side floating supply voltage (LF2113B)	V_B	-0.3	+624	V
High side floating supply offset voltage	V_S	V_B-24	V_B+0.3	V
High side floating output voltage	V_{HO}	V_S-0.3	V_B+0.3	V
Offset supply voltage transient	dV_s/dt	--	50	V/ns
Low side fixed supply voltage	V_{CC}	-0.3	+24	V
Low side output voltage	V_{LO}	-0.3	V_{CC}+0.3	V
Logic supply voltage	V_{DD}	-0.3	V_{SS}+24	V
Logic supply offset voltage	V_{SS}	V_{CC}-24	V_{CC}+0.3	V
Logic Input voltage (HIN, LIN & SD)	V_{IN}	V_{SS}-0.3	V_{DD}+0.3	V
Package power dissipation	P_D	--	1.25	W
Junction Temperature	T_J	--	+150	°C
Storage Temperature	T_{STG}	-55	+150	°C

Unless otherwise specified all voltages are referenced to COM . All electrical ratings are at $T_A = 25\,°C$

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

1.4 Thermal Characteristics

Parameter	Symbol	Rating	Units
Junction to ambient	θ_{jA}	100	° C/W

When mounted on a standard JEDEC 2-layer FR-4 board - JESD51-3

1.5 Recommended Operating Conditions

Parameter	Condition	Symbol	Min	Max	Unit
High side floating supply absolute voltage		V_B-V_S	10	20	V
High side floating supply offset voltage	LF2110B	V_S	Note1	500	V
	LF2113B		Note1	600	V
High side floating output voltage		V_{HO}	V_S	V_B	V
Low side fixed supply voltage		V_{CC}	10	20	V
Low side output voltage		V_{LO}	0	V_{CC}	V
Logic supply voltage		V_{DD}	V_{SS}+3	V_{SS}+20	V
Logic supply offset voltage	$V_{DD} \geq 5V$	V_{SS}	-5	5	V
	$V_{DD} < 5V$		- V_{DD}		
Logic Input voltage (HIN, LIN, SD)		V_{IN}	V_{SS}	V_{DD}	V
Ambient Temperature		T_A	-40	125	ºC

Unless otherwise specified all voltages are referenced to COM

NOTE1 *High-side driver remains operational for V_S transients down to -5V*

1.6 DC Electrical Characteristics

V_{CC}=V_{BS} =V_{DD} = 15V, T_A = 25 °C and V_{SS}= V_{COM} = 0V , unless otherwise specified.
The V_{IN} and I_{IN} parameters are applicable to all three logic input pins: HIN, LIN and SD. The V_O and I_O parameters are applicable to the respective output pins: HO and LO and are referenced to V_{COM}

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Logic "1" input voltage	V_{IH}	***NOTE 2***	9.5	--	--	V
Logic "0" input voltage	V_{IL}		--	--	5.0	V
Logic input voltage hysteresis	$V_{IN(HYS)}$	--	--	0.3	--	V
High level output voltage, V_{BIAS} - V_O	V_{OH}	I_O = 0A	--	--	1.4	V
Low level output voltage, V_O	V_{OL}	I_O = 20mA	--	--	0.15	V
Offset supply leakage current LF2110B / LF2113B	I_{LK}	V_B = V_S = 500V/600V	--	--	50	µA
Quiescent V_{BS} supply current	I_{BSQ}	V_{IN} = 0V or V_{DD}	--	55	230	µA
Quiescent V_{CC} supply current	I_{CCQ}	V_{IN} = 0V or V_{DD}	--	56	340	µA
Quiescent V_{DD} supply current	I_{DDQ}	V_{IN}= 0V or V_{DD}	--	0.6	30	µA
Logic "1" input bias current	I_{IN+}	V_{IN} = V_{DD}	--	20	40	µA
Logic "0" input bias current	I_{IN-}	V_{IN} = V_{SS}	--	--	5.0	µA
V_{BS} UVLO off positive going threshold	V_{BSUV+}	--	7.5	8.6	9.7	V
V_{BS} UVLO enable negative going threshold	V_{BSUV-}	--	7.0	8.2	9.4	V
V_{BS} UVLO hysteresis	$V_{BSUV(HYS)}$	--	--	0.3	--	V
V_{CC} UVLO off positive going threshold	V_{CCUV+}	--	7.4	8.5	9.6	V
V_{CC} UVLO enable negative going threshold	V_{CCUV-}	--	7.0	8.2	9.4	V
V_{CC} UVLO hysteresis	$V_{CCUV(HYS)}$	--	--	0.3	--	V
Output high short circuit pulsed current	I_{O+}	V_O = 0V, V_{IN} = V_{DD}, $t \leq 10$ µs	2.0	2.5	--	A
Output low short circuit pulsed current	I_{O-}	V_O = 15V, V_{IN} = 0V, $t \leq 10$ µs	2.0	2.5	--	A

NOTE 2 *For optimal operation, it is recommended the input pulse (to HIN and LIN) should have a minimum amplitude of 9.5V (V_{DD}=15V) with a minimum pulse width of 200ns .*

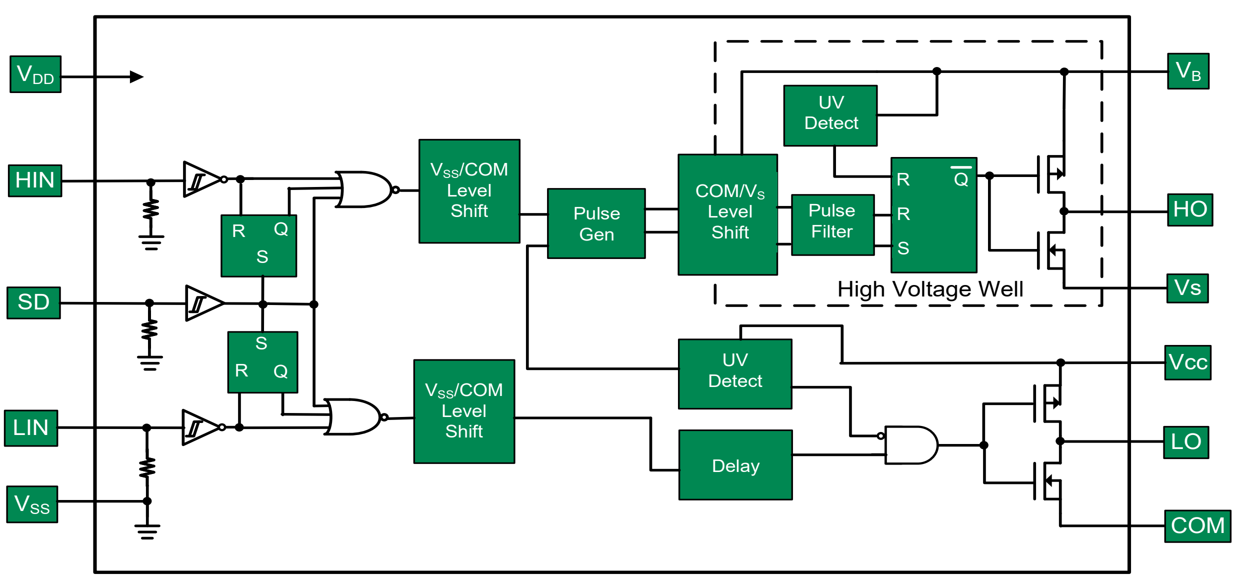
1.7 AC Electrical Characteristics

$V_{CC} = V_{BS} = V_{DD} = 15V$, $T_A = 25$ °C, $C_L = 1000pF$, and $V_{SS} = V_{COM} = 0V$ unless otherwise specified.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Turn-on propagation delay	t_{ON}	$V_S = 0V$	--	105	150	ns
Turn-off propagation delay	t_{OFF}	LF2110B: $V_S = 500V$ LF2113B: $V_S = 600V$	--	94	125	ns
Shut down propagation delay	t_{SD}	LF2110B: $V_S = 500V$ LF2113B: $V_S = 600V$	--	70	140	ns
Turn-on rise time	t_r	--	--	15	35	ns
Turn-off fall time	t_f	--		13	25	ns
Propagation Delay Matching	t_{DM}	LF2110B	--	--	10	ns
		LF2113B	--	--	20	ns

2 Functional Description

2.1 Functional Block Diagram



2.2 Timing Waveforms

Figure 1. Input / Output Logic Diagram

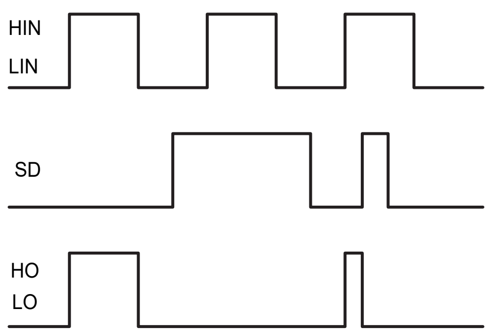


Figure 2. Input-to-Output Delay Timing Diagram

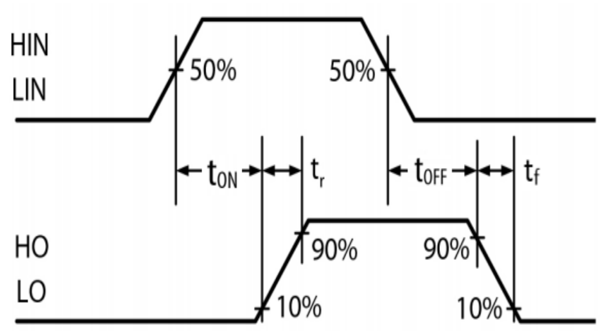


Figure 3. Shutdown Timing Diagram

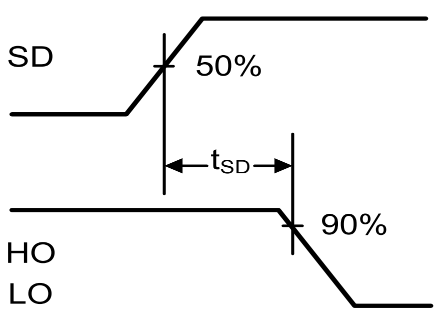
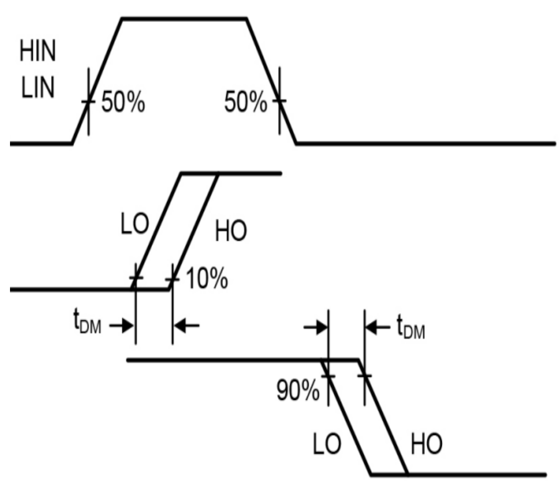


Figure 4. Propagation Delay Matching Diagram



2.3 Application Information

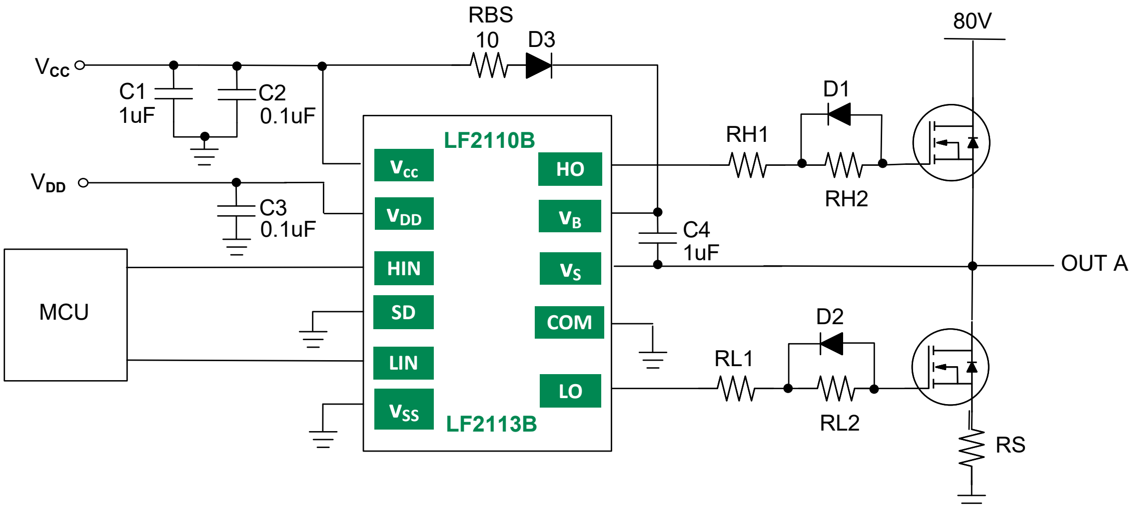


Figure 5. Single phase (of four) for Stepper motor driver application using the LF2110B / LF2113B

- RH1 and RL1 value is typically between 5Ω and 10Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 10Ω is used in this example.
- It is **highly recommended** that the input pulse (to HIN and LIN) should have a minimum amplitude of 9.5V (for VDD=15V) with a minimum pulse width of 200ns.
- RH2 and RL2 value is typically between 20Ω and 100Ω, exact value decided by MOSFET junction capacitance and drive current of gate driver; 50Ω is used in this example.
- D3 is rated at 1000V, 1A. Use Diodes Inc. US1M or equivalent .

3 Performance Data

Unless otherwise noted $V_{CC} = V_{BS} = V_{DD} = 12V$, $T_A = 25\ °C$, $V_{SS} = V_{COM} = 0V$ and values are typical.

Figure 6. Turn-on Propogation Delay vs. Supply Voltage

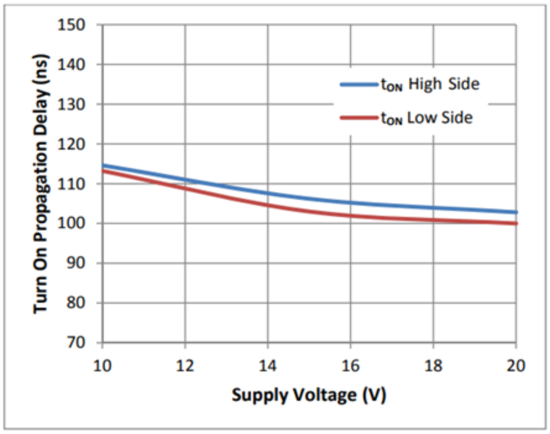


Figure 7. Turn-on Propogation Delay vs. Temperature

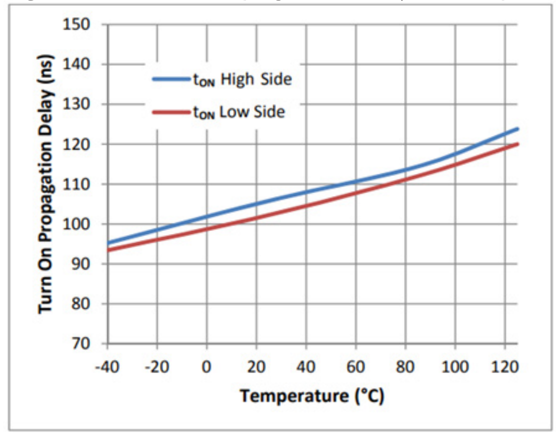


Figure 8. Turn-off Propogation Delay vs. Supply Voltage

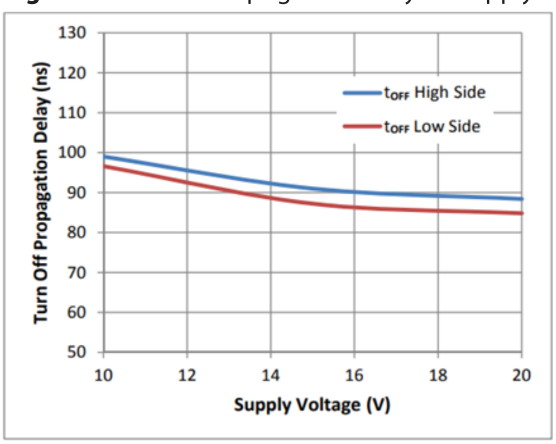


Figure 9. Turn-off Propogation Delay vs. Temperature

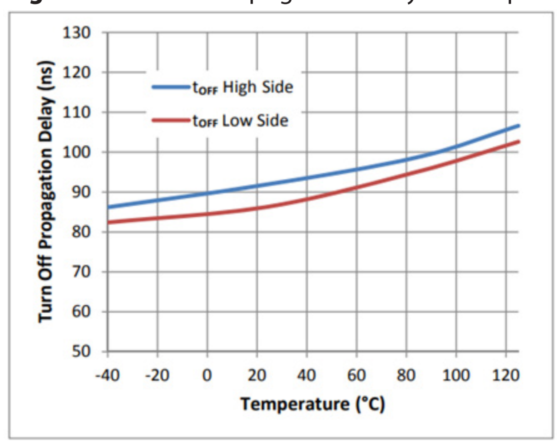


Figure 10. Rise Time vs. Supply Voltage

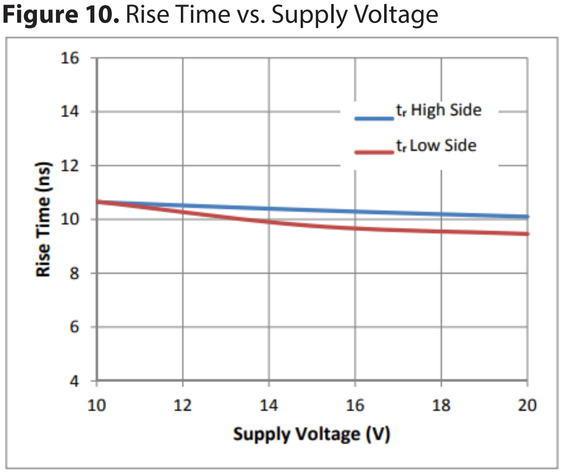


Figure 11. Rise Time vs. Temperature

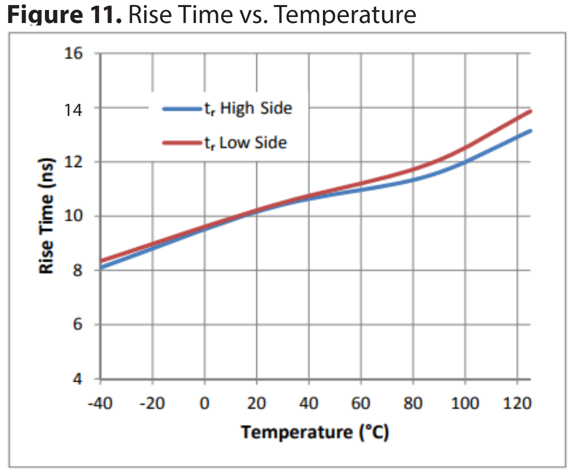


Figure 12. Fall Time vs. Supply Voltage

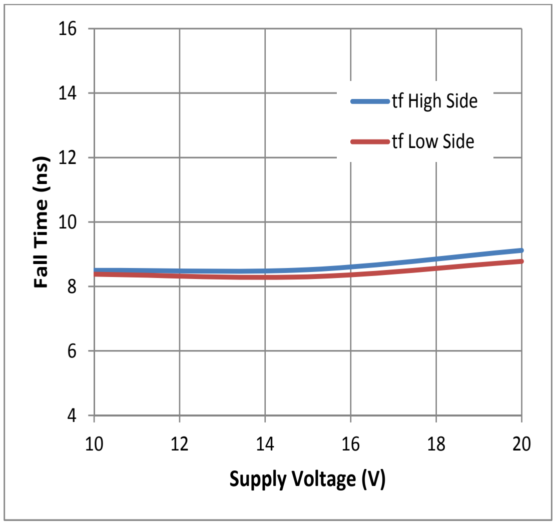


Figure 13. Fall Time vs. Temperature

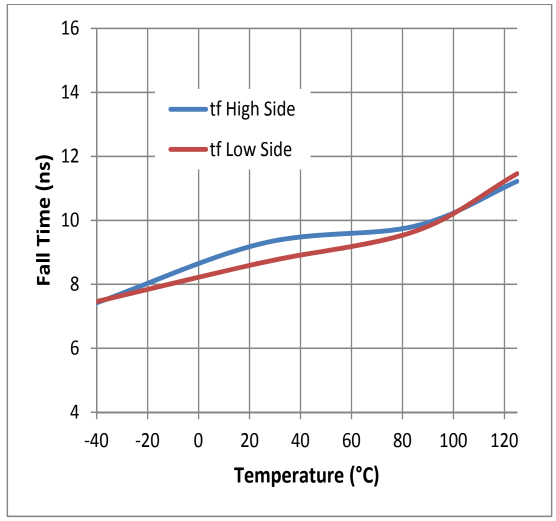


Figure 14. Quiescent Current vs. Supply Voltage

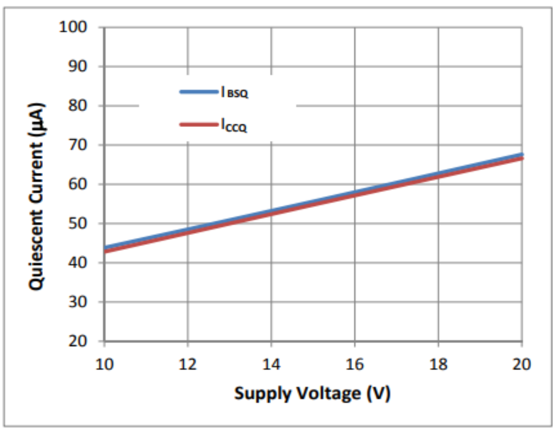


Figure 15. Quiescent Current vs. Temperature

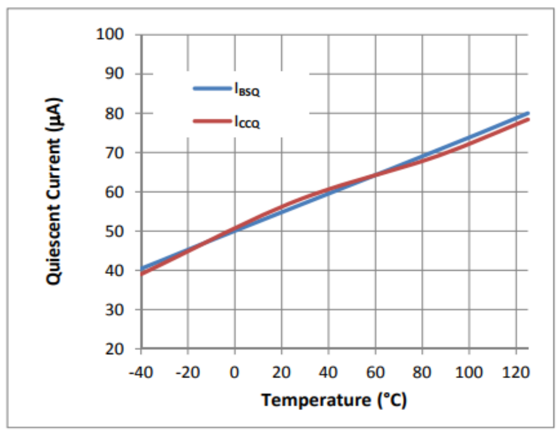


Figure 16. Delay Matching vs. Supply Voltage

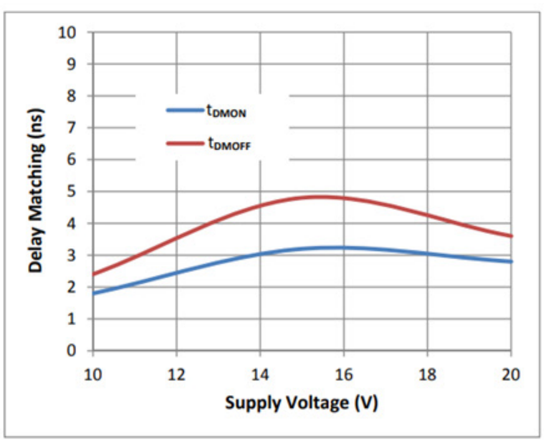


Figure 17. Delay Matching vs. Temperature

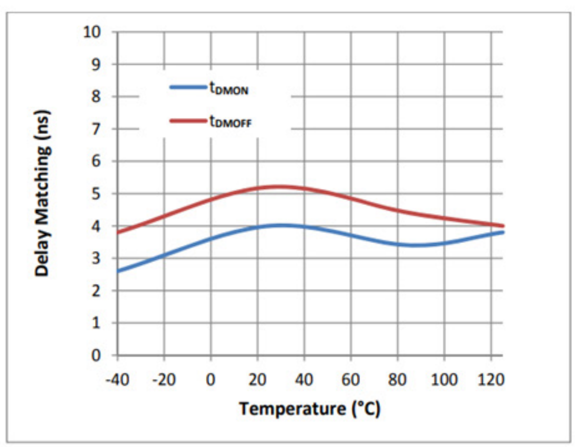


Figure 18. Output Source Current vs. Supply Voltage

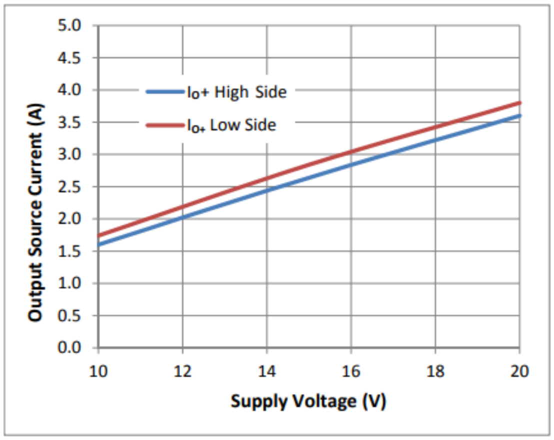


Figure 19. Output Source Current vs. Temperature

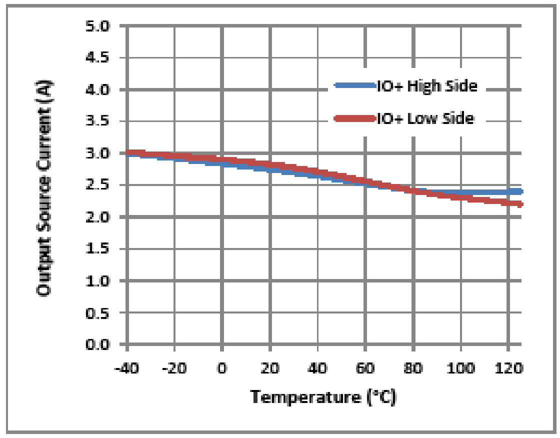


Figure 20. Output Sink Current vs. Supply Voltage

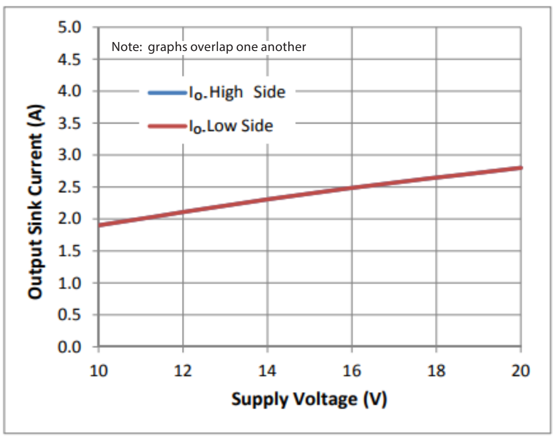


Figure 21. Output Sink Current vs. Temperature

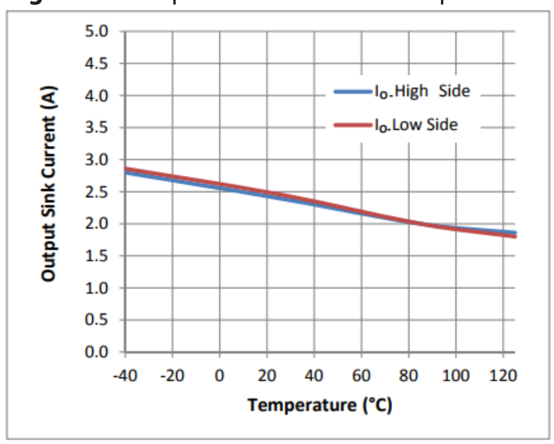


Figure 22. Logic 1 Input Voltage vs. Supply Voltage

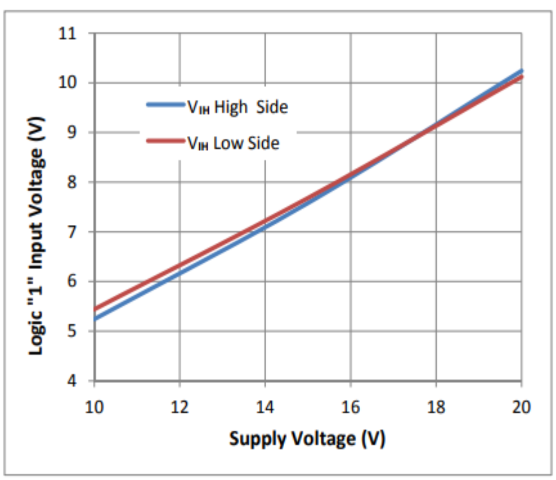


Figure 23. Logic 1 Input Voltage vs. Temperature

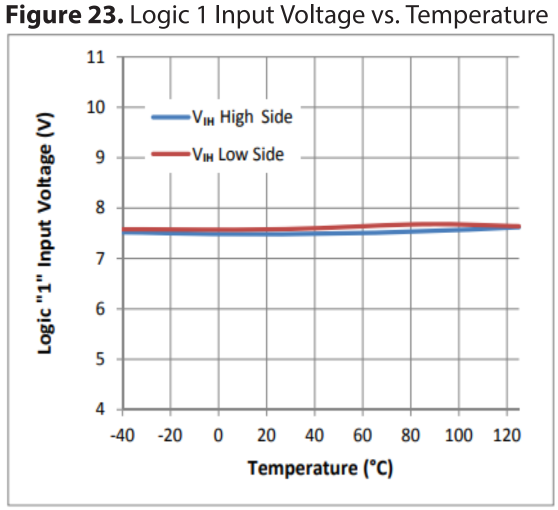


Figure 24. Logic 0 Input Voltage vs. Supply Voltage

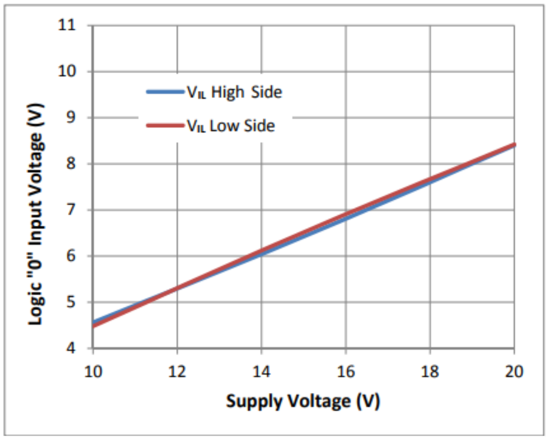


Figure 25. Logic 0 Input Voltage vs. Temperature

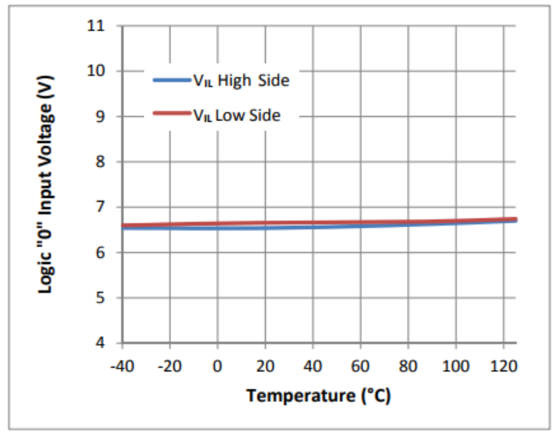


Figure 26. V_{CC} UVLO vs. Temperature

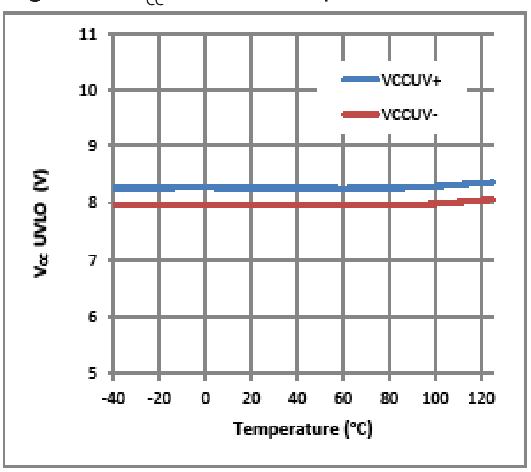


Figure 27. V_{BS} UVLO vs. Temperature

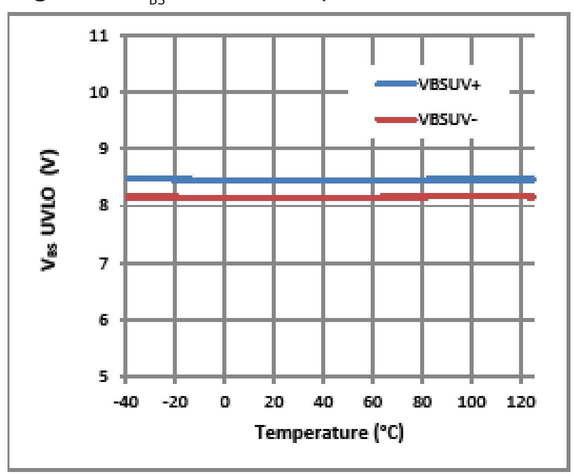


Figure 28. Offset Supply Leakage Current vs. Temperature

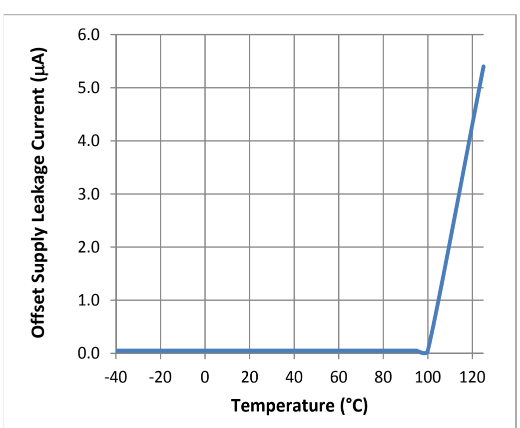


Figure 29. V_S Maximum Offset vs. Supply Voltage

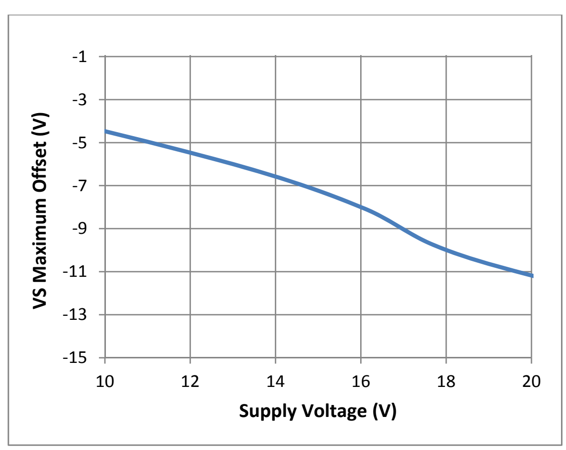


Figure 30. Input Bias Current vs. Temperature

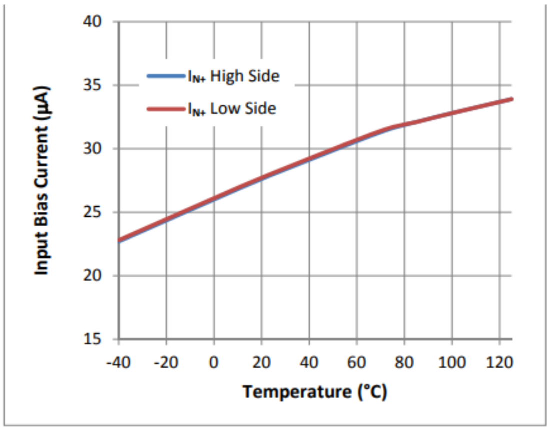
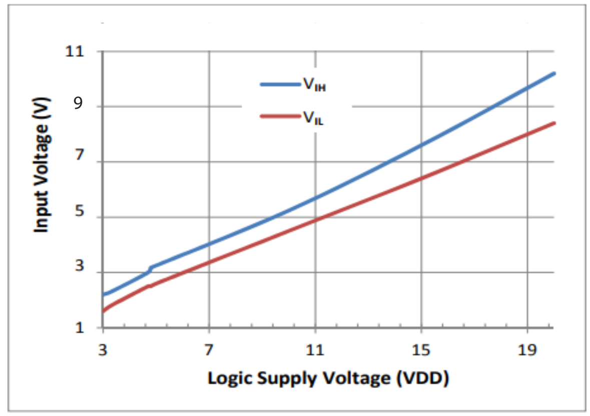


Figure 31. Input Voltage Threshold vs. V_{DD}



4 Manufacturing Information

4.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. Littelfuse Integrated Circuits Division classified all of its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** rating as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033.**

Device	Moisture Sensitivity Level (MSL) Classification
LF2110B , LF2113B	MSL3

4.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

4.3 Reflow Profile

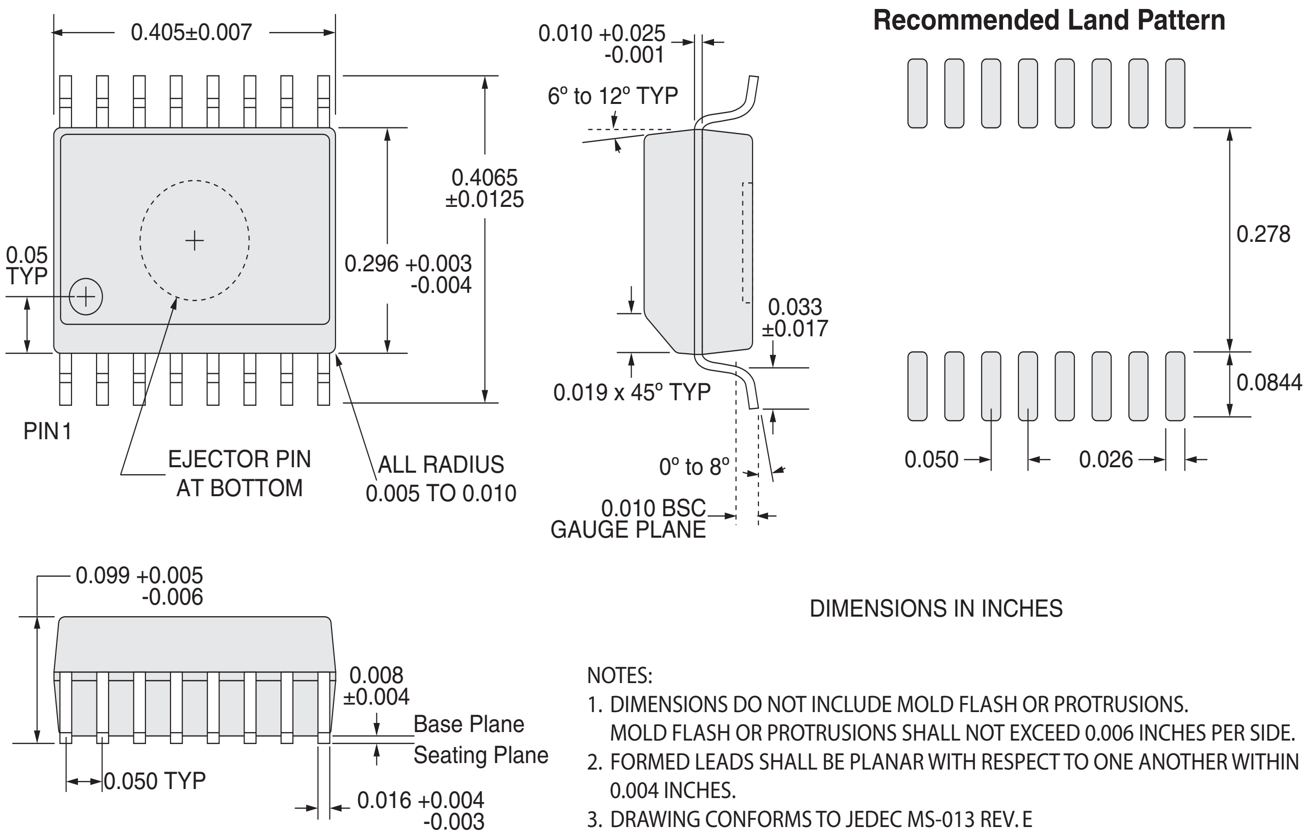
Provided in the table below is the IPC/JEDEC J-STD-020 Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

Device	Classification Temperature(Tc)	Dwell Time (tp)	Max Reflow Cycles
LF2110B, LF2113B	260°C	30 seconds	3

4.4 Board Wash

Littelfuse recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

5 Package Dimensions (SOIC-16)



DIMENSIONS IN INCHES

NOTES:
1. DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
   MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
2. FORMED LEADS SHALL BE PLANAR WITH RESPECT TO ONE ANOTHER WITHIN 0.004 INCHES.
3. DRAWING CONFORMS TO JEDEC MS-013 REV. E

Important Notice

Disclaimer Notice - Information furnished is believed to be accurate and reliable. However, users should independently evaluate the suitability of and test each product selected for their own applications. Littelfuse products are not designed for, and may not be used in, all applications. Read complete Disclaimer Notice at **https://www.littelfuse.com/disclaimer-electronics**.