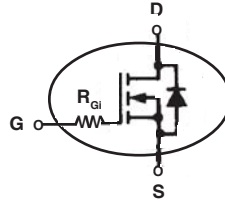


Power MOSFET with Extended FBSOA

IXTH30N50L
IXTQ30N50L
IXTT30N50L

N-Channel Enhancement Mode



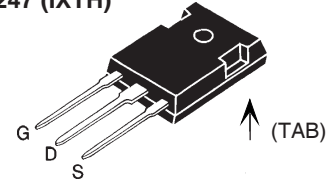
$$V_{DSS} = 500V$$

$$I_{D25} = 30A$$

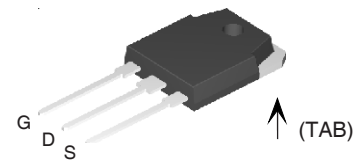
$$R_{DS(on)} \leq 0.20\Omega$$

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	500	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	500	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ C$	30	A
I_{DM}	$T_C = 25^\circ C$, pulse width limited by T_{JM}	60	A
I_{AR}	$T_C = 25^\circ C$	30	A
E_{AR}	$T_C = 25^\circ C$	50	mJ
E_{AS}		1.5	J
P_D	$T_C = 25^\circ C$	400	W
T_J		-55 to +150	$^\circ C$
T_{JM}		+150	$^\circ C$
T_{stg}		-55 to +150	$^\circ C$
T_L	1.6mm (0.063in) from case for 10s	300	$^\circ C$
T_{SOLD}	Plastic body for 10s	260	$^\circ C$
M_d	Mounting torque (TO-247, TO-3P)	1.13/10	Nm/lb.in.
Weight	TO-247	6.0	g
	TO-3P	5.5	g
	TO-268	5.0	g

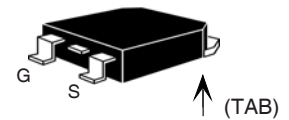
TO-247 (IXTH)



TO-3P (IXTQ)



TO-268 (IXTT)



G = Gate D = Drain
S = Source TAB = Drain

Features

- Designed for linear operation
- International standard packages
- Unclamped Inductive Switching (UIS) rated.
- Molding epoxies meet UL 94 V-0 flammability classification
- Integrated gate resistor for easy paralleling
- Guaranteed FBSOA at $75^\circ C$

Applications

- Solid state circuit breakers
- Soft start controls
- Linear amplifiers
- Programmable loads
- Current regulators

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
$(T_J = 25^\circ C, \text{ unless otherwise specified})$				
BV_{DSS}	$V_{GS} = 0V, I_D = 250\mu A$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	2.5		4.5 V
I_{GSS}	$V_{GS} = \pm 30V, V_{DS} = 0V$			± 100 nA
I_{DSS}	$V_{DS} = V_{DSS}$			50 μA
	$V_{GS} = 0V$			300 μA
$R_{DS(on)}$	$V_{GS} = 10V, I_D = 0.5 \cdot I_{D25}$, Note 1			0.20 Ω

Symbol	Test Conditions	Characteristic Values			
		Min.	Typ.	Max.	
$(T_J = 25^\circ\text{C}, \text{ unless otherwise specified})$					
g_{fs}	$V_{DS} = 10\text{V}, I_D = 0.5 \cdot I_{D25}, \text{ Note 1}$	9	12	15	S
C_{iss}	$V_{GS} = 0\text{V}, V_{DS} = 25\text{V}, f = 1\text{MHz}$		10.2		nF
C_{oss}			540		pF
C_{rss}			127		pF
R_{Gi}	Integrated gate input resistor		3.5		Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$ $R_G = 0\Omega \text{ (External)}$		35		ns
t_r			117		ns
$t_{d(off)}$			94		ns
t_f			40		ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}, V_{DS} = 0.5 \cdot V_{DSS}, I_D = 0.5 \cdot I_{D25}$		240		nC
Q_{gs}			58		nC
Q_{gd}			135		nC
R_{thJC}				0.31	$^\circ\text{C/W}$
R_{thCS}	(TO-247, TO-3P)	0.25			$^\circ\text{C/W}$

Safe Operating Area Specification

Symbol	Test Conditions	Min.	Typ.	Max.
SOA	$V_{DS} = 400\text{V}, I_D = 0.5\text{A}, T_C = 75^\circ\text{C}, t_p = 2\text{s}$	200		W

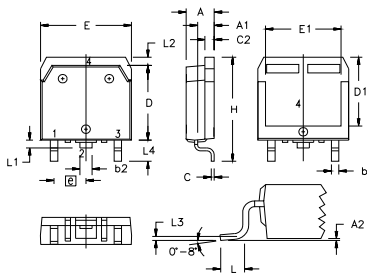
Source-Drain Diode

Characteristic Values
($T_J = 25^\circ\text{C}, \text{ unless otherwise specified}$)

Symbol	Test Conditions	Min.	Typ.	Max.	
I_s	$V_{GS} = 0\text{V}$			30	A
I_{SM}	Repetitive, pulse width limited by T_{JM}			120	A
V_{SD}	$I_F = I_s, V_{GS} = 0\text{V}, \text{ Note 1}$			1.5	V
t_{rr}	$I_F = I_s, -di/dt = 100\text{A}/\mu\text{s}, V_R = 100\text{V}$		500		ns

Note 1: Pulse test, $t \leq 300\mu\text{s}$; duty cycle, $d \leq 2\%$.

TO-268 (IXTT) Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.193	.201	4.90	5.10
A1	.106	.114	2.70	2.90
A2	.001	.010	0.02	0.25
b	.045	.057	1.15	1.45
b2	.075	.083	1.90	2.10
C	.016	.026	0.40	0.65
C2	.057	.063	1.45	1.60
D	.543	.551	13.80	14.00
D1	.488	.500	12.40	12.70
E	.624	.632	15.85	16.05
E1	.524	.535	13.30	13.60
e	.215 BSC		5.45 BSC	
H	.736	.752	18.70	19.10
L	.094	.106	2.40	2.70
L1	.047	.055	1.20	1.40
L2	.039	.045	1.00	1.15
L3	.010 BSC		0.25 BSC	
L4	.150	.161	3.80	4.10

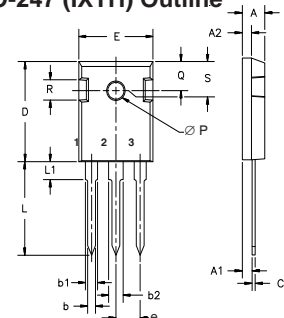
PRELIMINARY TECHNICAL INFORMATION

The product presented herein is under development. The Technical Specifications offered are derived from data gathered during objective characterizations of preliminary engineering lots; but also may yet contain some information supplied during a pre-production design evaluation. IXYS reserves the right to change limits, test conditions, and dimensions without notice.

IXYS reserves the right to change limits, test conditions, and dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,850,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

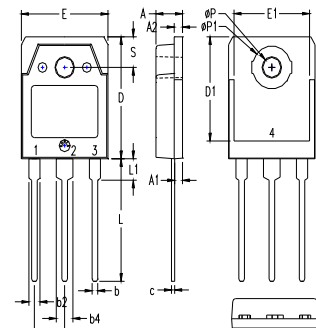
TO-247 (IXTH) Outline



Terminals: 1 - Gate
2 - Drain
3 - Source
Tab - Drain

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.7	5.3	.185	.209
A ₁	2.2	2.54	.087	.102
A ₂	2.2	2.6	.059	.098
b	1.0	1.4	.040	.055
b ₁	1.65	2.13	.065	.084
b ₂	2.87	3.12	.113	.123
C	.4	.8	.016	.031
D	20.80	21.46	.819	.845
E	15.75	16.26	.610	.640
e	5.20	5.72	0.205	0.225
L	19.81	20.32	.780	.800
L1		4.50		.177
$\varnothing P$	3.55	3.65	.140	.144
S	5.89	6.40	0.232	0.252
R	4.32	5.49	.170	.216
S	6.15	BSC	242	BSC

TO-3P (IXTQ) Outline



1 - GATE
2 - DRAIN (COLLECTOR)
3 - SOURCE (EMITTER)
4 - DRAIN (COLLECTOR)

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.193	4.70	4.90
A1	.051	.059	1.30	1.50
A2	.057	.065	1.45	1.65
b	.035	.045	0.90	1.15
b2	.075	.087	1.90	2.20
b4	.114	.126	2.90	3.20
c	.022	.031	0.55	0.80
D	.780	.799	19.80	20.30
D1	.665	.677	16.90	17.20
E	.610	.622	15.50	15.80
E1	.531	.539	13.50	13.70
e	.215 BSC		5.45 BSC	
L	.779	.795	19.80	20.20
L1	.134	.142	3.40	3.60
$\varnothing P$.126	.134	3.20	3.40
$\varnothing P1$.272	.280	6.90	7.10
S	.193	.201	4.90	5.10

Fig. 1. Output Characteristics
@ $T_J = 25^\circ\text{C}$

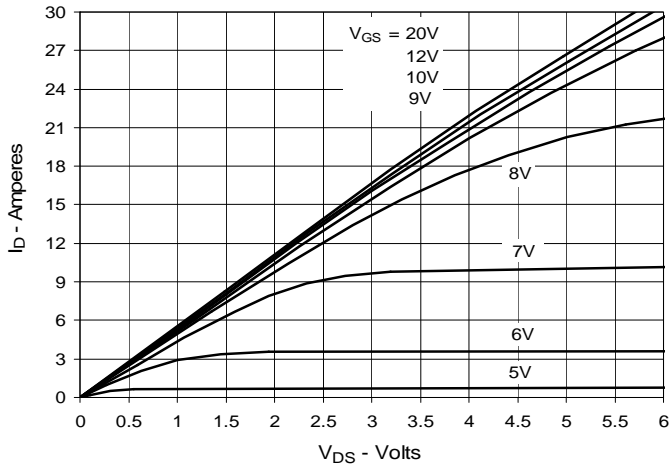


Fig. 2. Extended Output Characteristics
@ $T_J = 25^\circ\text{C}$

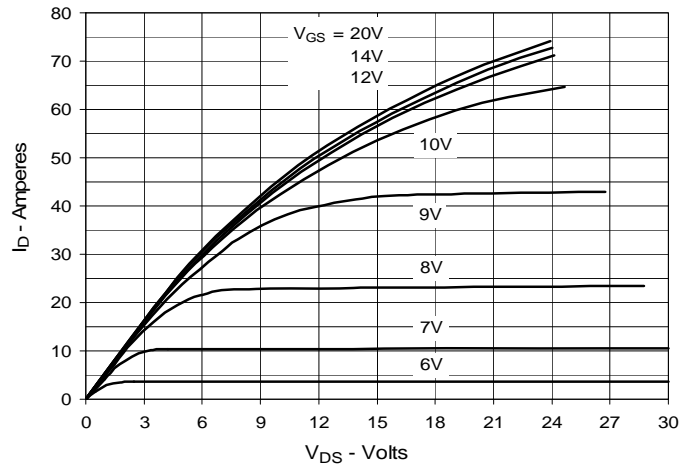


Fig. 3. Output Characteristics
@ $T_J = 125^\circ\text{C}$

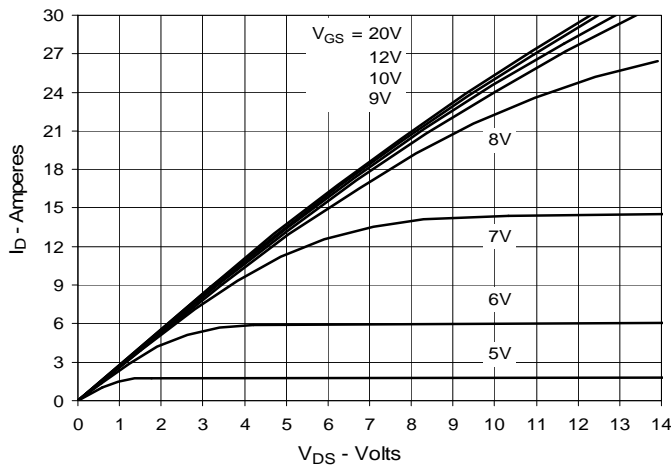


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 15\text{A}$ Value vs. Junction Temperature

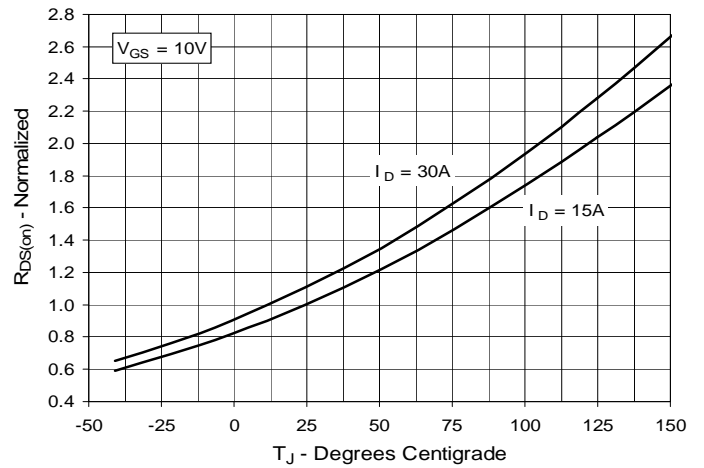


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 15\text{A}$ Value vs. Drain Current

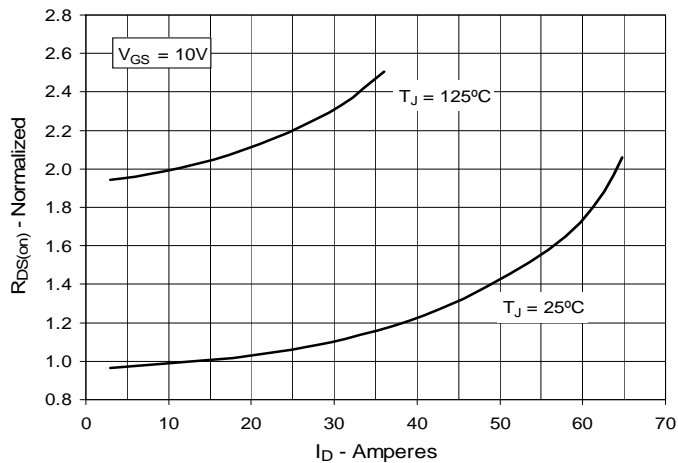


Fig. 6. Maximum Drain Current vs. Case Temperature

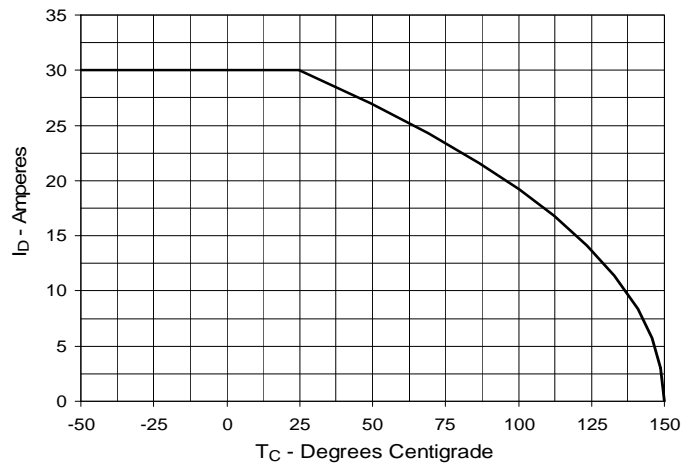


Fig. 7. Input Admittance

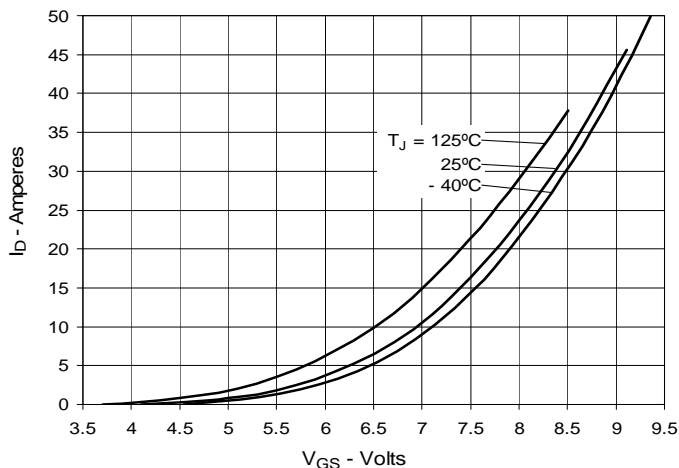


Fig. 8. Transconductance

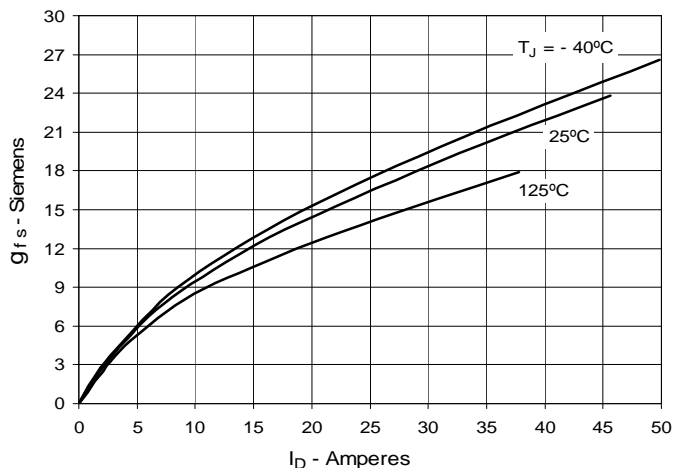


Fig. 9. Forward Voltage Drop of Intrinsic Diode

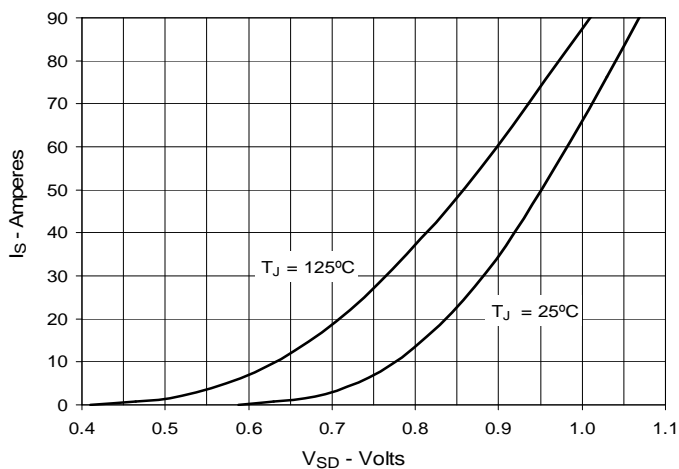


Fig. 10. Gate Charge

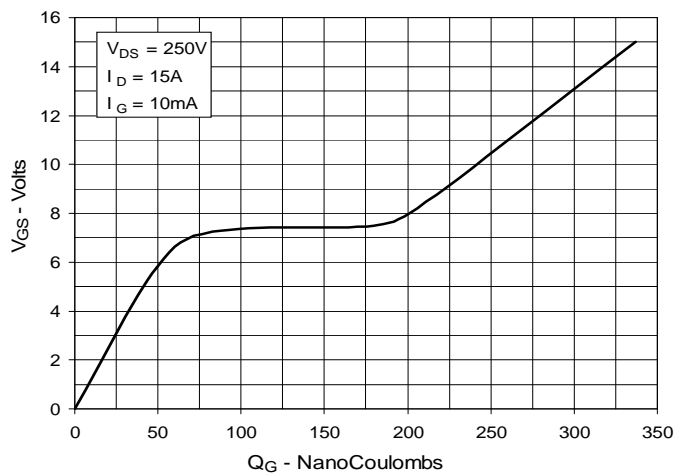


Fig. 11. Capacitance

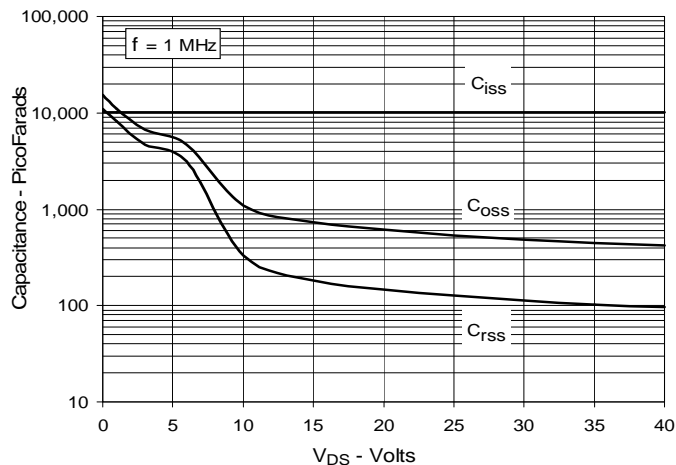


Fig. 12. Maximum Transient Thermal Impedance

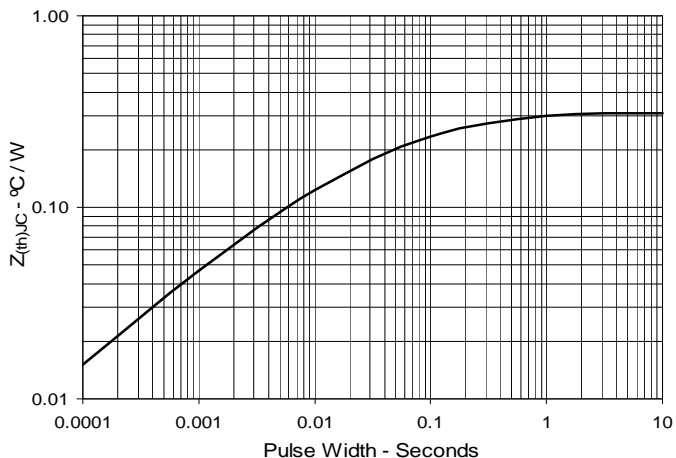


Fig. 13. Forward-Bias Safe Operating Area
@ $T_C = 25^\circ\text{C}$

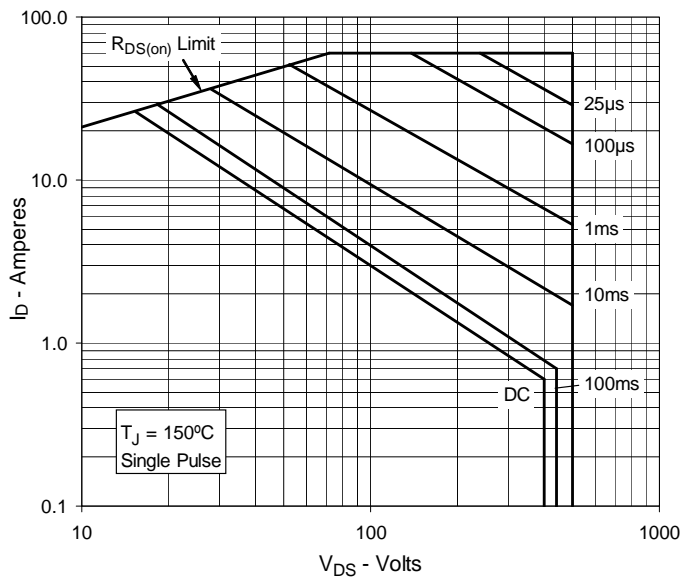
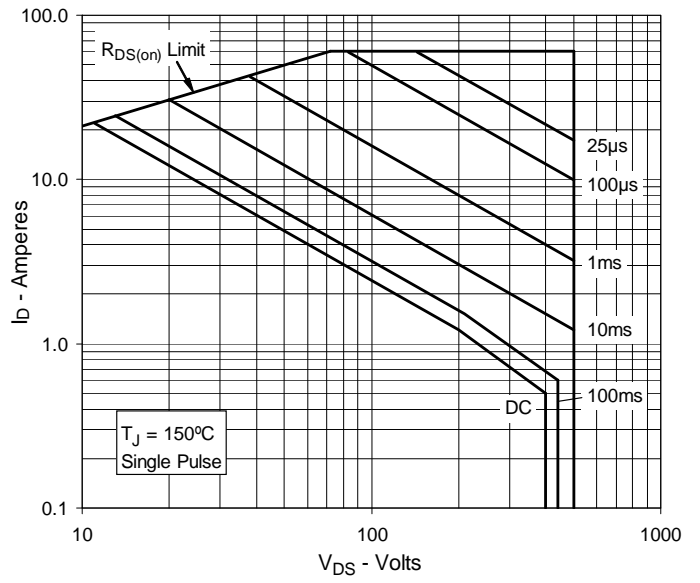


Fig. 14. Forward-Bias Safe Operating Area
@ $T_C = 75^\circ\text{C}$





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