

# Depletion Mode MOSFET

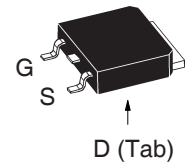
**IXTY01N100D**  
**IXTU01N100D**  
**IXTP01N100D**

$V_{DSX} = 1000V$   
 $R_{DS(on)} \leq 80\Omega$

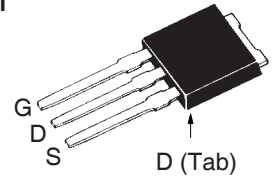
N-Channel



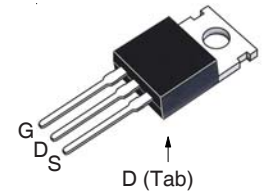
TO-252  
(IXTY)



TO-251  
(IXTU)



TO-220  
(IXTP)



G = Gate    D = Drain  
S = Source    Tab = Drain

Symbol	Test Conditions	Maximum Ratings	
$V_{DSX}$	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	1000	V
$V_{DGX}$	$T_J = 25^\circ\text{C to } 150^\circ\text{C}$	1000	V
$V_{GSX}$	Continuous	$\pm 20$	V
$V_{GSM}$	Transient	$\pm 30$	V
$I_{DM}$	$T_C = 25^\circ\text{C}$ , Pulse Width Limited by $T_J$	400	mA
$P_D$	$T_C = 25^\circ\text{C}$	25	W
	$T_A = 25^\circ\text{C}$	1.1	W
$T_J$		- 55 ... +150	$^\circ\text{C}$
$T_{JM}$		150	$^\circ\text{C}$
$T_{stg}$		- 55 ... +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
$T_{SOLD}$	1.6 mm (0.062in.) from Case for 10s	260	$^\circ\text{C}$
$M_d$	Mounting Torque (TO-220)	1.13 / 10	Nm/lb.in.
Weight	TO-252	0.35	g
	TO-251	0.40	g
	TO-220	3.00	g

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$BV_{DSX}$	$V_{GS} = -10V$ , $I_D = 25\mu\text{A}$	1000		V
$V_{GS(off)}$	$V_{DS} = 25V$ , $I_D = 25\mu\text{A}$	- 2.0		- 4.5 V
$I_{GSX}$	$V_{GS} = \pm 20V$ , $V_{DS} = 0V$			$\pm 100$ nA
$I_{DSX(off)}$	$V_{DS} = V_{DSX}$ , $V_{GS} = -10V$ $T_J = 125^\circ\text{C}$			10 $\mu\text{A}$ 250 $\mu\text{A}$
$R_{DS(on)}$	$V_{GS} = 0V$ , $I_D = 50\text{mA}$ , Note 1		50	80 $\Omega$
$I_{D(on)}$	$V_{GS} = 0V$ , $V_{DS} = 25V$ , Note 1		400	mA

## Features

- Normally ON Mode
- International Standard Packages
- Low  $R_{DS(on)}$  HDMOS™ Process
- Rugged Polysilicon Gate Cell Structure
- Fast Switching Speed

## Advantages

- Easy to Mount
- Space Savings
- High Power Density

## Applications

- Level Shifting
- Triggers
- Solid State Relays
- Current Regulators

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$g_{fs}$	$V_{DS} = 100\text{V}$ , $I_D = 100\text{mA}$ , Note 1	100	200	mS
$C_{iss}$	$V_{GS} = -10\text{V}$ , $V_{DS} = 25\text{V}$ , $f = 1\text{MHz}$		100	pF
$C_{oss}$			12	pF
$C_{rss}$			2	pF
$t_{d(on)}$	<b>Resistive Switching Times</b> $V_{GS} = \pm 5\text{V}$ , $V_{DS} = 50\text{V}$ , $I_D = 50\text{mA}$ $R_G = 30\Omega$ (External)		7	ns
$t_r$			10	ns
$t_{d(off)}$			34	ns
$t_f$			64	ns
$Q_{g(on)}$	$V_{GS} = \pm 5\text{V}$ , $V_{DS} = 500\text{V}$ , $I_D = 50\text{mA}$		5.8	nC
$Q_{gs}$			3.6	nC
$Q_{gd}$			0.4	nC
$R_{thJC}$	TO-220			5.0 $^\circ\text{C/W}$
$R_{thCS}$		0.50		$^\circ\text{C/W}$

#### Source-Drain Diode

Symbol	Test Conditions ( $T_J = 25^\circ\text{C}$ , Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$V_{SD}$	$I_F = 100\text{mA}$ , $V_{GS} = -10\text{V}$ , Note 1			1.5 V
$t_{rr}$	$I_F = 750\text{mA}$ , $-di/dt = 100\text{A}/\mu\text{s}$ $V_R = 25\text{V}$ , $V_{GS} = -10\text{V}$			1.5 $\mu\text{s}$

Note 1. Pulse test,  $t \leq 300\mu\text{s}$ , duty cycle,  $d \leq 2\%$ .

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:

4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

Fig. 1. Output Characteristics @  $T_J = 25^\circ\text{C}$

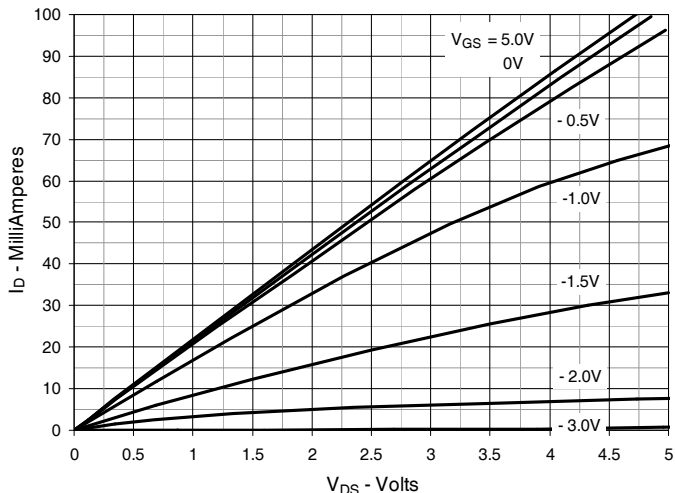


Fig. 2. Output Characteristics @  $T_J = 125^\circ\text{C}$

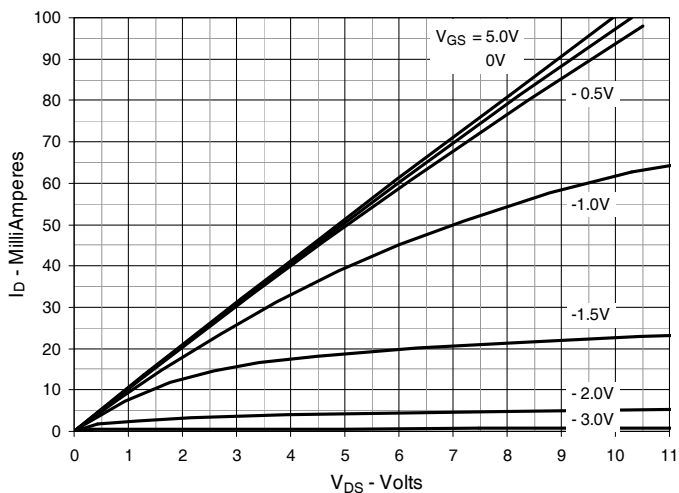


Fig. 3. Drain Current @  $T_J = 25^\circ\text{C}$

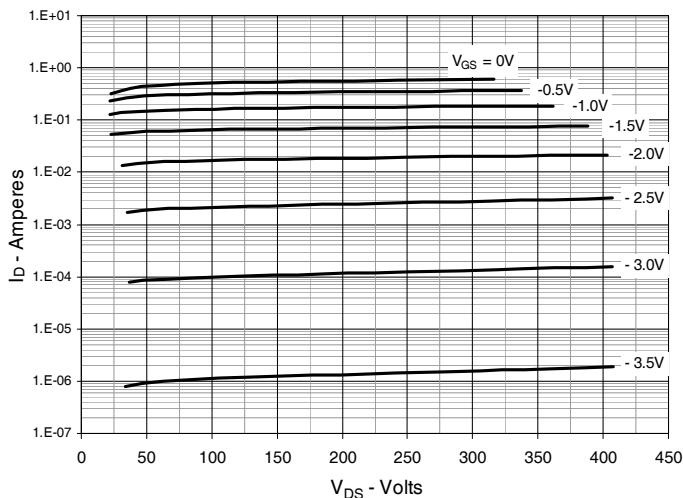


Fig. 4. Drain Current @  $T_J = 100^\circ\text{C}$

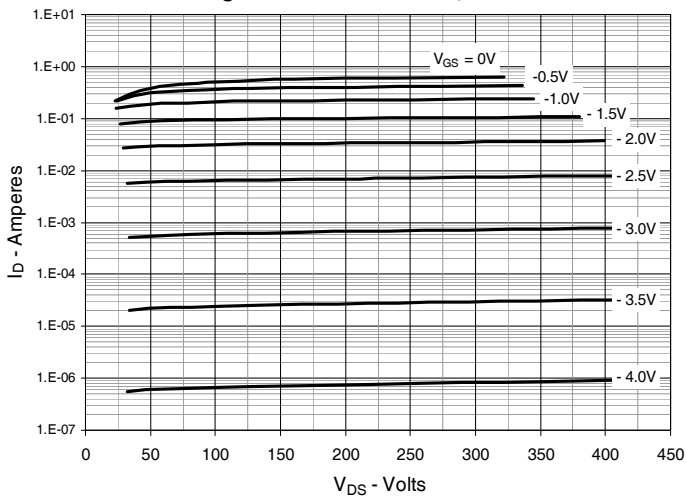


Fig. 5. Dynamic Resistance vs. Gate Voltage

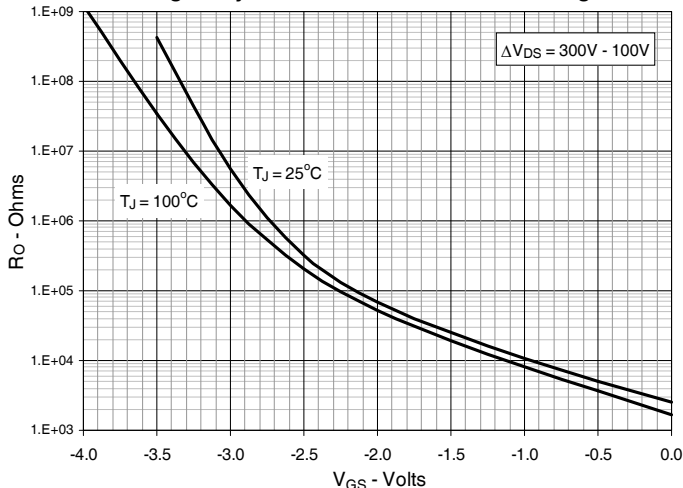
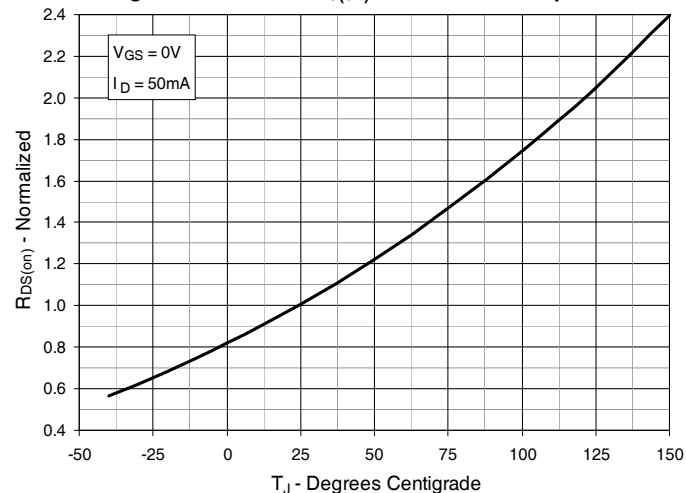
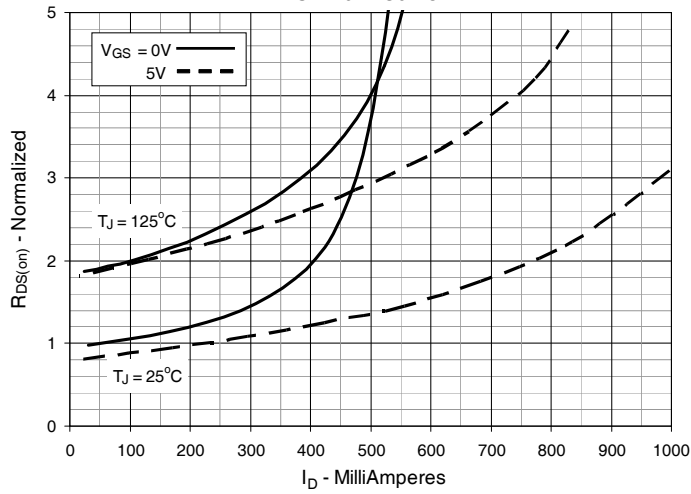


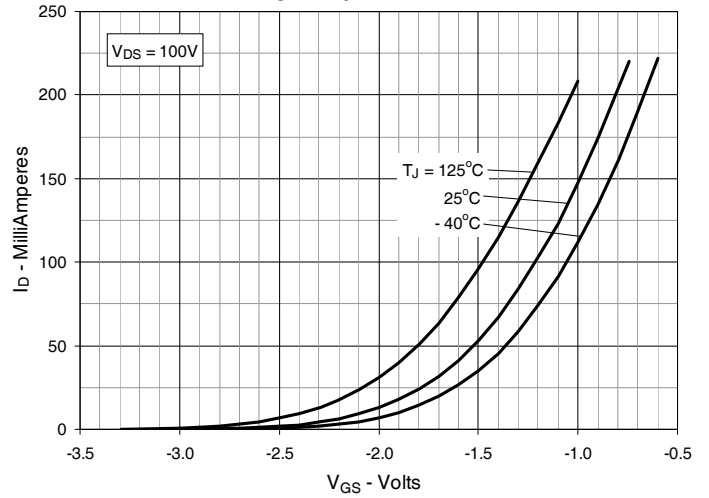
Fig. 6. Normalized  $R_{DS(on)}$  vs. Junction Temperature



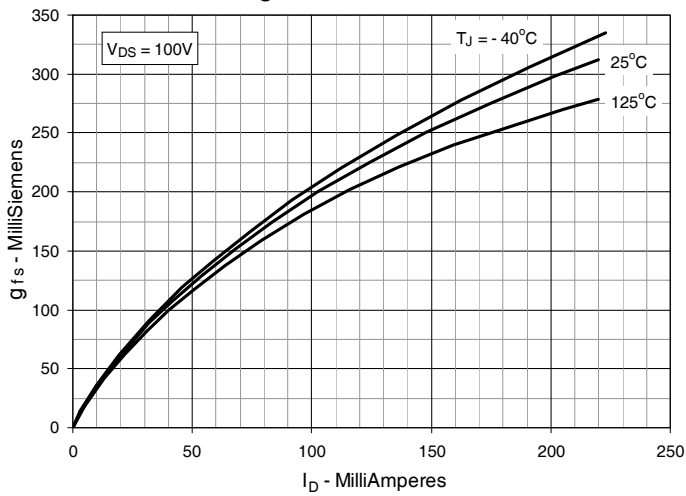
**Fig. 7.  $R_{DS(on)}$  Normalized to  $I_D = 50mA$  Value vs. Drain Current**



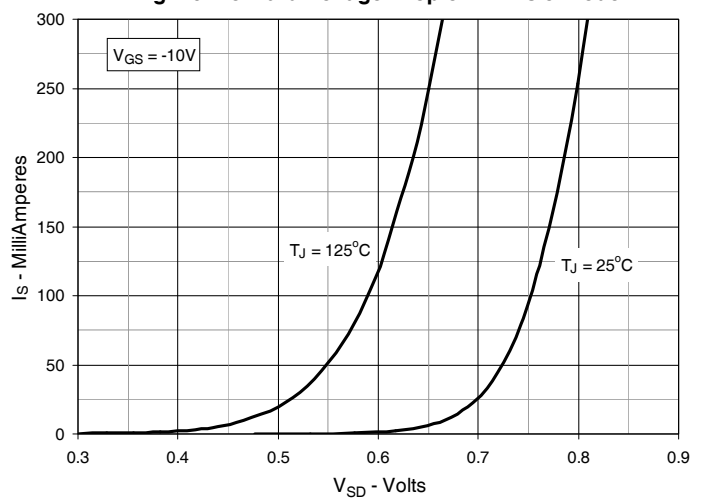
**Fig. 8. Input Admittance**



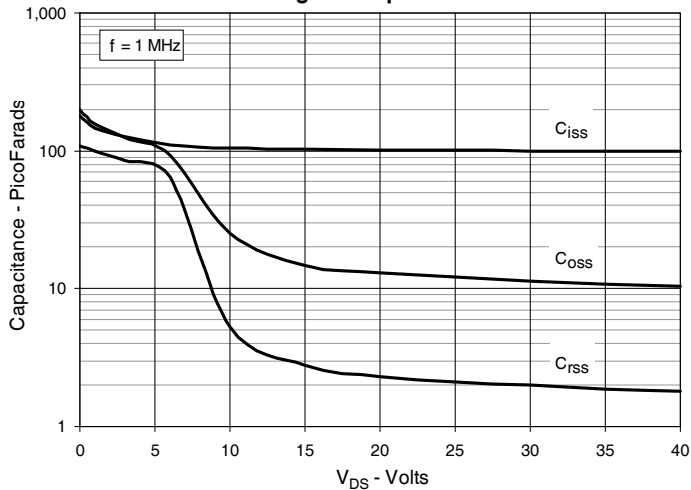
**Fig. 9. Transconductance**



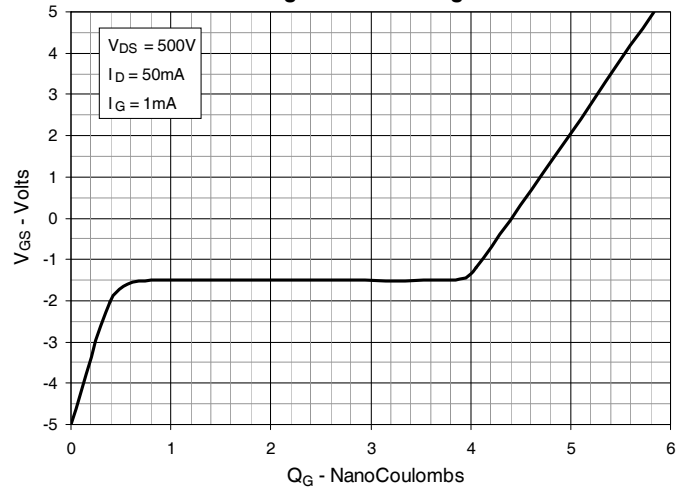
**Fig. 10. Forward Voltage Drop of Intrinsic Diode**



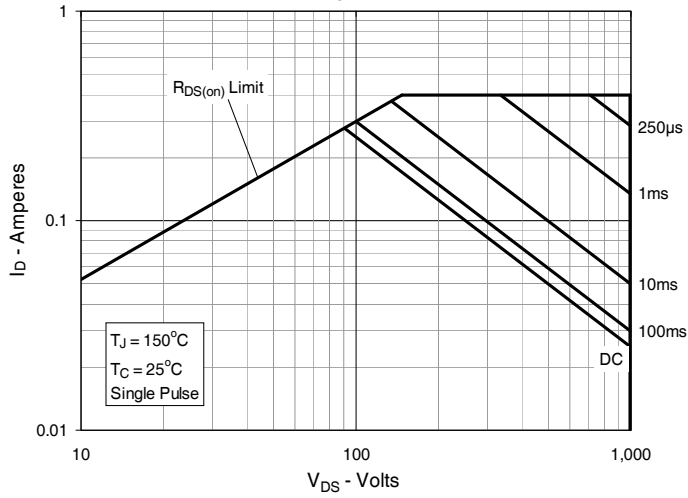
**Fig. 11. Capacitance**



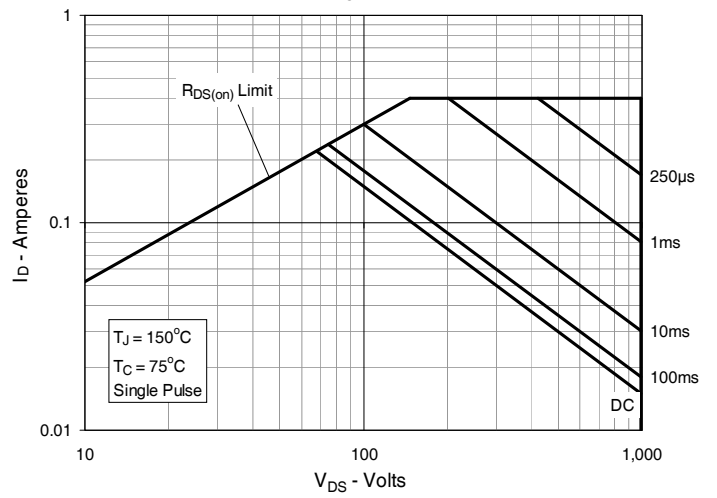
**Fig. 12. Gate Charge**



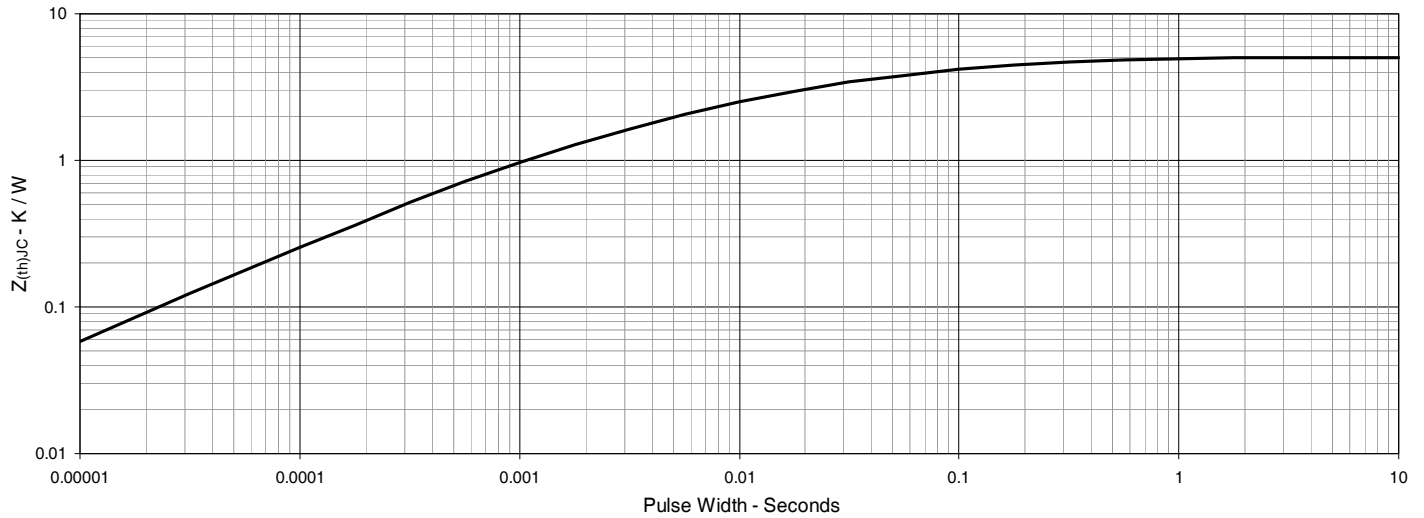
**Fig. 13. Forward-Bias Safe Operating Area**  
@  $T_C = 25^\circ\text{C}$



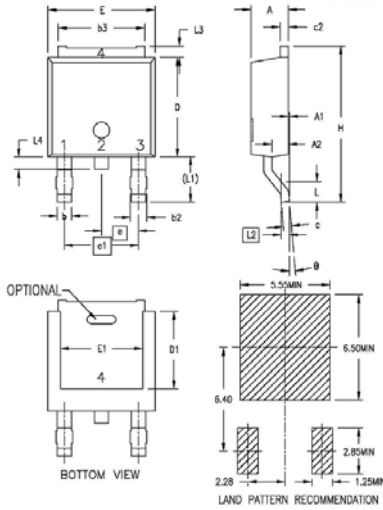
**Fig. 14. Forward-Bias Safe Operating Area**  
@  $T_C = 75^\circ\text{C}$



**Fig. 15. Maximum Transient Thermal Impedance**



### TO-252 Outline

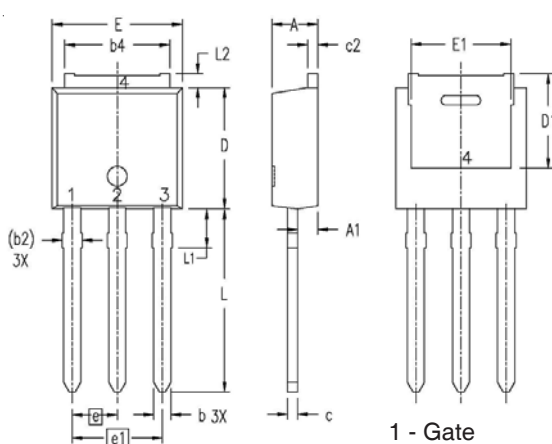


1 - Gate  
2,4 - Drain  
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.086	.094	2.19	2.38
A1	0	.005	0	0.12
A2	.038	.046	0.97	1.17
b	.025	.035	0.64	0.89
b2	.030	.045	0.76	1.14
b3	.200	.215	5.08	5.46
c	.018	.024	0.46	0.61
c2	.018	.023	0.46	0.58
D	.235	.245	5.97	6.22
D1	.180	.205	4.57	5.21
E	.250	.265	6.35	6.73
E1	.170	.205	4.32	5.21
e	.090 BSC		2.28 BSC	
e1	.180 BSC		4.57 BSC	
H	.370	.410	9.40	10.42
L	.055	.070	1.40	1.78
L1	.100	.115	2.54	2.92
L2	.020 BSC		0.50 BSC	
L3	.025	.040	0.64	1.02
L4	.025	.040	0.64	1.02
θ	0°		10°	

NOTE: 1. This drawing comply JEDEC TO-252AA value except L3 dimension.  
2. All metal surface are tin plated except trimmed area.

### TO-251 Outline

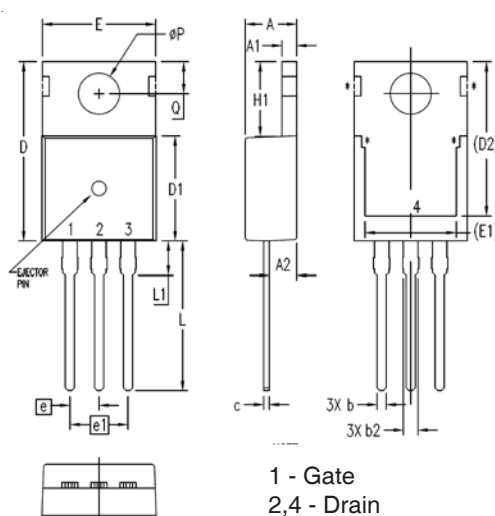


1 - Gate  
2,4 - Drain  
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.087	.094	2.20	2.40
A1	.032	.048	0.82	1.22
b	.026	.034	0.66	0.86
(b2)	.030	.038	0.76	0.96
b4	.198	.222	5.04	5.64
c	.018	.024	0.45	0.60
c2	.016	.024	0.40	0.60
D	.232	.248	5.90	6.30
(D1)	.179	.195	4.55	4.95
E	.252	.268	6.40	6.80
(E1)	.191	.207	4.85	5.25
e	.090 BSC		2.28 BSC	
e1	.180 BSC		4.57 BSC	
L	.358	.374	9.10	9.50
L1	.063	.079	1.60	2.00
L2	.020	.035	0.50	0.90

NOTE: 1. ALL METAL AREA ARE MATTE PURE TIN PLATED EXCEPT TRIMMED AREA.  
2. THESE DIMENSIONS DO NOT INCLUDE PROTRUSIONS OF THE MOLD.  
3. THE ( ) MARK IS THE REFERENCE ONLY.

### TO-220 Outline



1 - Gate  
2,4 - Drain  
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.169	.185	4.30	4.70
A1	.047	.055	1.20	1.40
A2	.079	.106	2.00	2.70
b	.024	.039	0.60	1.00
b2	.045	.057	1.15	1.45
c	.014	.026	0.35	0.65
D	.587	.626	14.90	15.90
D1	.335	.370	8.50	9.40
(D2)	.500	.531	12.70	13.50
E	.382	.406	9.70	10.30
(E1)	.283	.323	7.20	8.20
e	.100 BSC		2.54 BSC	
e1	.200 BSC		5.08 BSC	
H1	.244	.268	6.20	6.80
L	.492	.547	12.50	13.90
L1	.110	.154	2.80	3.90
ØP	.134	.150	3.40	3.80
Q	.106	.126	2.70	3.20

NOTE: 1. All metal surface are matte pure tin plated except trimmed area.



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