60 W Auxiliary Power Supply

Design Summary

Objectives

This application note describes the design and performance of a 60 W auxiliary power supply with wide input voltage for industrial applications using 1.7 kV 1 ohm SiC MOSFETs from Littelfuse. The evaluation board was designed to evaluate the performance of part number LSIC1MO170E0750 for ease of use.

Design Features

Features of the Auxiliary Power Supply Evaluation Board include:

- Single-switch fly-back topology
- Closed loop control output voltage regulation
- High power conversion efficiency over a wide power range
- 300 V~1000 V wide input voltage

Applications

- Motor drives
- PV inverters
- UPS Systems
- Modular Multilevel Converter

Target Audience

This document is intended for potential adopters of the LSIC1MO170E0750 interested in designing low cost and high-performance systems of off-line SMPS for auxiliary power supply for industrial applications.

Contact Information

For more information on the topic of auxiliary power supplies, contact the Littelfuse Power Semiconductor team of product and applications experts:

- PowerSemiSupport@Littelfuse.com

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1. Introduction

Auxiliary power supply has become an essential part of electronic devices in multiple industrial applications such as motor drives, PV inverters, UPS systems, and modular multilevel converters. The common high voltage DC link or bus is used to provide a low voltage (5 V~48 V) source for powering equipment such as control circuits, sensing circuits, and cooling fans. Galvanic isolation is a common requirement for such power supplies and the power level is usually below 100 W. These auxiliary power supplies are required to operate from a wide input voltage range, typically from 300 V up to 1000 V, due to the DC link voltage variation. A simple low-complexity design with high reliability is required to ensure that the auxiliary supply does not become a limiting factor to system reliability. Single-switch fly-back topology is the most common selection for this type of low-power DC-DC power conversion due to its simple structure, lowest component count, and low cost. However, there are several challenges to the selection of silicon MOSFETs for a single-switch fly-back topology for auxiliary power supply applications. In a fly-back topology, the power switching device must have the voltage capability to withstand a total system voltage of highest input supply, transformer induced effects, secondary reflected voltage, and circuit arrangement/layout effects.

At 1000 V input, the peak voltage on a power switching device can be easily over 1200 V, which makes it difficult to select a silicon MOSFET with proper blocking voltages. A 1500 V Si MOSFET will have low margin and raise reliability concerns. Si MOSFETs rated 2000 V and above can provide sufficient margin, but the specific on-state resistance is much higher than lower voltage MOSFETs which will reduce converter efficiency and compromise heat management. This consequence may necessitate larger cooling solutions even for a low power conversion application. In addition, the cost of 2000+ V rated Si MOSFETs is much higher. To utilize Si MOSFETs rated 1500 V and lower, two-switch fly-back or other topologies should be used. In a two-switch fly-back topology however, the design complexity and converter component counts will increase significantly.

The introduction of 1700 V SiC MOSFETs provides a possible solution by using simple single-switch fly-back topology for such applications to achieve a wide input voltage range. **Figure 1** presents the topology of a single-switch fly-back converter for auxiliary power supply applications using a 1700 V SiC MOSFET.

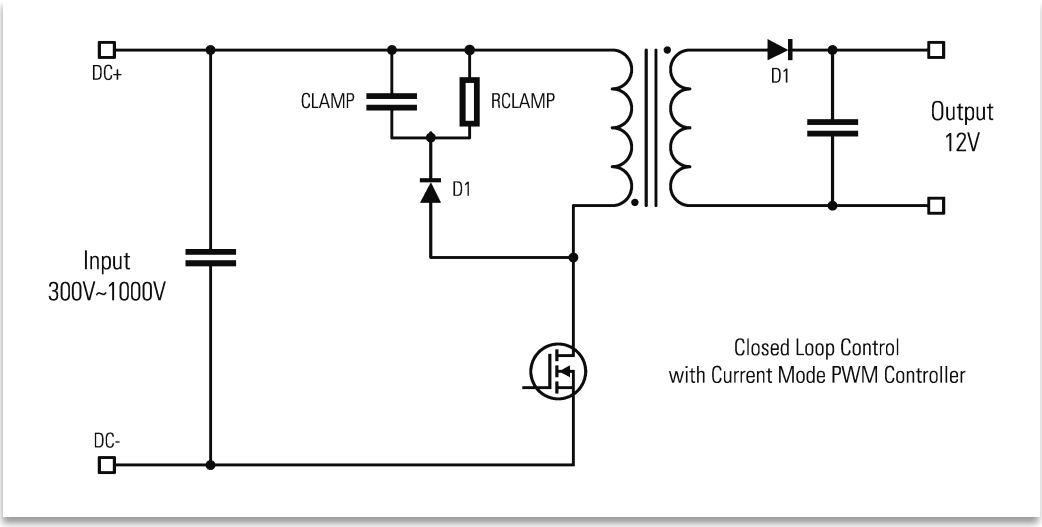

Figure 1. Single Switch Fly-back Converter for Auxiliary Power Supply Applications

The 1700 V breakdown voltage provides enough voltage margin even for 1000 V input voltage. The specific ON resistance of 1700 V SiC MOSFETs is much lower than that of 2000 V and above rated Si MOSFETs. Therefore, smaller packages can be used for the same ON resistance rating thereby improving the cost-performance of a 1700 V SiC MOSFET. Additionally, SiC MOSFETs have lower switching losses compared to Si MOSFETs, which can improve converter efficiency and reduce the size of the heatsink or even remove the need for a heatsink. Lower switching losses also provide an option to increase switching frequency of the auxiliary power supply to reduce transformer size and weight.

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2. Evaluation Board

Figure 2 shows an image of the evaluation board hardware. Several key parts, including the DC-link capacitor, decoupling capacitor, SiC MOSFET, isolation transformer, output rectifier, driver IC, analog closed-loop circuit, and connectors are displayed.

Figure 2. Evaluation Board Hardware

2.1. Evaluation Board Specifications

Table 1 lists the electrical specifications of the evaluation board.

Table 1. Electrical Specifications of Evaluation Board

Specifications	Value
Minimum Input Voltage (V_{IN_MIN})	300 V
Maximum Input Voltage (V_{IN_MAX})	1000 V
Output Voltage (V_{OUT})	12 V
Output Voltage Ripple (V_{OUT_RIPPLE})	<10 mV
Maximum Output Current (I_{OUT_MAX})	5 A
Maximum Output Power (P_{OUT_MAX})	60 W
Switching Frequency (F_S)	110 kHz
Efficiency (>20% Load)	>80%
Peak Efficiency (E_{FF_MAX})	86%

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3. Schematic

Figure 3 displays the schematic of the evaluation board. The power stage circuit includes the DC link capacitor, RCD snubber/clamping circuit, isolation transformer, SiC MOSFETs, gate driving circuit, sensing resistor, and output rectification circuit. Control circuits include the controller IC and its configuration components, voltage closed-loop feedback circuit, and the control power supply circuit. The design and parameter selection method is discussed in the next section.

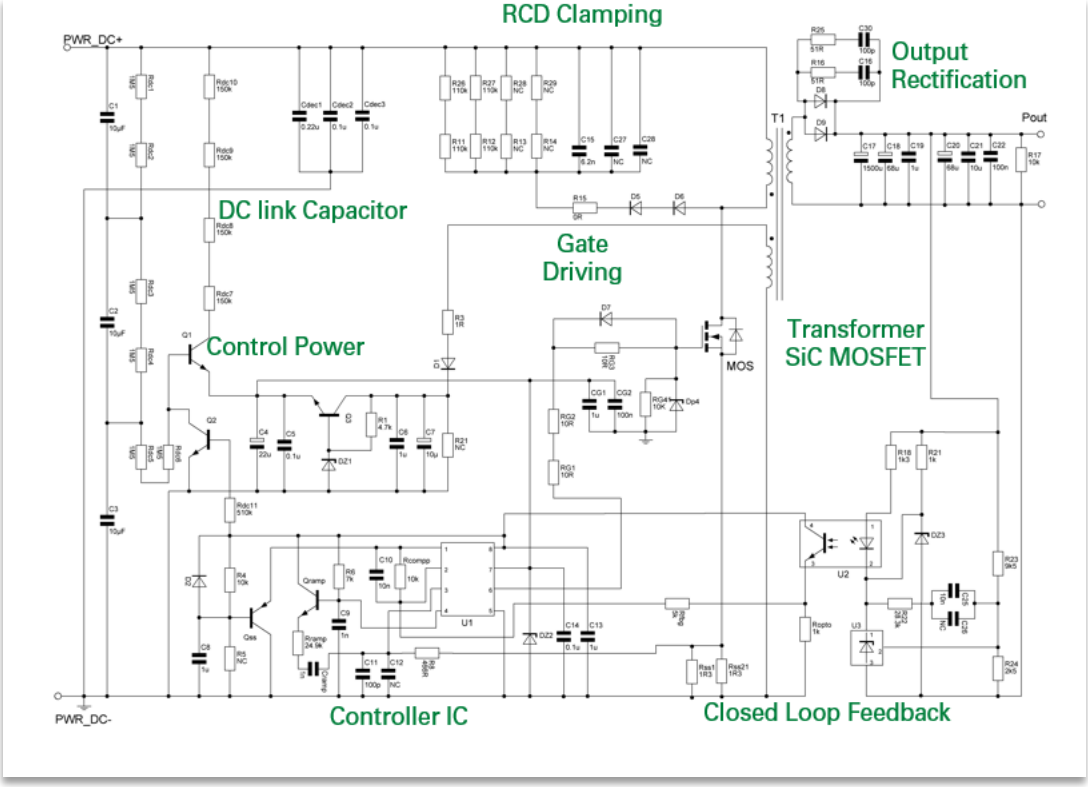

Figure 3. Evaluation Board Schematic Diagram

4. Circuit Design

4.1. Power Stage Main Component Selection

4.1.1. Primary Side Switching Device

The 1700 V 1ohm SiC MOSFET, housed in an industry standard three lead TO-247 package from Littelfuse (Part Number LSIC1MO170E0750) was selected as the primary side switching power device. Considering the maximum 1000 V input and the reflected voltages at the transformer from secondary side 12 V output voltage, the device peak voltage can reach more than 1200 V. The 1700 V break down voltage can provide sufficient margin for design optimization. Meanwhile, the low switching loss energy and ultra-low gate charge of SIC MOSFETs enable higher switching frequencies for a more compact transformer design with lower power loss. The TO-247 package also provides a large surface area and lower R_{THC-A} for simpler thermal management compared to smaller outline packages for low voltage devices.

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4.1.2. Transformer Turns Ratio

The primary to secondary turns ratio (Np-Ns) of the transformer will determine the real peak voltage on the primary side MOSFET and secondary side rectification diode. For a 1700 V MOSFET, 85% derating is recommended, considering a maximum leakage inductance voltage spike of 25% of the maximum input voltage. The maximum allowed reflected voltage from secondary side can be estimated as:

$$V_{refl\_max} = 0.85 \times V_{BV} - 1.3 \times V_{in} = 195V$$

Considering a V_F = 0.7 V forward voltage drop of the output rectification diode, the maximum turns ratio for 12 V output voltage can be calculated as:

$$N_{PS} = \frac{V_{refl\_max}}{V_{out} + V_F} = 15.35$$

A turns ratio of N_{PS} = 12 is selected in the evaluation board design.

4.1.3. Secondary Side Rectification Diode

The output rectification diode peak voltage is equal to the output voltage plus the reflected input voltage, as shown in the following equation:

$$V_{diode} = \frac{V_{in\_max}}{N_{PS}} + V_{out} = 95V$$

A 150 V diode from IXYS is selected as the rectification diode.

4.1.4. Switching Frequency

The switching frequency of the power converter is one of the most important design parameters as it influences factors such as switching losses, transformer losses, overall converter size/weight, and converter level Electromagnetic Interference (EMI). Compared to Si switches, SiC MOSFETs have low switching loss energy and ultra-low gate charge, which enables a higher switching frequency for a more compact transformer design with lower power loss. For this evaluation board, a switching frequency of f_s=110 kHz was selected considering the overall optimization of converter loss.

4.1.5. Transformer Inductance

To avoid high peak current and avoid false protection triggering, the evaluation converter is designed to operate in Continuous Conduction Mode (CCM) at high load conditions. The minimum value of the magnetizing inductance of the transformer to maintain the converter in CCM mode is determined by the input voltage, switching frequency, and the CCM working range. Higher magnetizing inductance can extend the CCM condition to reduce semiconductor loss and reduce power stage EMI noise emission. However, it will require more turns on the transformer, increasing the weight and leakage inductance. In fly-back converters, high leakage will increase the power loss in the RCD clamping circuit because all the energy stored in the leakage inductance needs to be dissipated as power loss. Therefore, magnetizing inductance of the transformer cannot be too large. In this sample design, the CCM operation mode is designed between 50% and 100% load range at maximum input voltage. Therefore, the transformer primary side inductance can be calculated as:

$$L_{P\_min} = \frac{{V_{in\_min}}^2 \times \left(\frac{N_{ps} \times V_{out}}{V_{in\_min} + N_{ps} \times V_{out}}\right)^2}{2 \times 50\% \times P_{in} \times f_s} = 1.18mH$$

In the equation above, P_{in} is the estimated input power, considering the maximum output power and estimated efficiency.

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An inductance of L_P = 1.2 mH is selected in this design. Based on the selected inductance and switching frequency, the current stress on power devices can be calculated as follows:

$$I_{MOS\_Max} = \frac{P_{in}}{V_{in\_min} \times \frac{N_{ps} \times V_{out}}{V_{in\_min} + N_{ps} \times V_{out}}} + \frac{V_{in\_min}}{2 \times L_P \times f_s} \times \frac{N_{ps} \times V_{out}}{V_{in\_min} + N_{ps} \times V_{out}}$$

In the equation above, the peak current is 1.2 A.

The actual design and implementation of the transformer is presented in the following sections.

4.1.6. Output Capacitance

The minimum value for output capacitance is determined by the ripple requirement for output voltage. In this example, a <10 mV output ripple is required for 12 V output voltage, then the minimum capacitance value can be calculated as:

$$C_{out\_min} = \frac{V_{out}}{V_{out\_ripple}} \times \frac{I_{out} \times \frac{N_{ps} \times V_{out}}{V_{in\_min} + N_{ps} \times V_{out}}}{V_{in\_min} \times f_s}$$

The output capacitance is selected as 1700 µF and consists of one 1500 µF aluminum capacitor and several SMD ceramic capacitors to filter voltages ripple noise at different frequency.

4.2. Controller IC Configuration

4.2.1. Controller IC Selection

A wide selection of IC controllers is available for industrial auxiliary power supply applications. For this application note, the TI UCCx8C4x family current mode PWM controller was selected. To select the proper device part number, the UVLO protection level and maximum duty cycle need to be calculated. Considering the relative high gate driving voltage requirement of SiC MOSFETs, high UVLO protection function is preferred. The maximum duty cycle of the sample converter can be calculated from the voltage transfer function of a CCM fly-back converter, as shown below.

$$D_{max} = \frac{N_{ps} \times V_{out}}{V_{in\_min} + N_{ps} \times V_{out}} = 0.3369$$

Because the D_{max} value is less than 50%, part number UCC28C44 was selected for this evaluation board design.

4.2.2. Auxiliary Circuit for IC Configuration

To ensure the proper operation of the driver IC, the power supply voltage for the driver IC must exceed the UVLO limitation (14.5 V) and a proper decoupling capacitor is required to bypass high frequency noise on the power line. The decoupling capacitor (0.1 uF) should be placed right under the power pin of the driver IC. It is recommended that a 20 V Zener diode be connected between the IC power pin and ground for protection.

The switching frequency of PWM signals is configurated by the values of the capacitor and resistor that are connected to the RT/CT pin (Pin4). A 1 nF capacitor and 7 kOhm resistor are used to obtain a switching frequency of 110 kHz. The use of a CP0 ceramic capacitor and high precision chip resistor is recommended to ensure that the switching frequency is maintained under different ambient temperatures.

The driver IC creates a 5 V reference voltage. A 1 µF decoupling capacitor is recommended right under the VREF pin of the driver IC.

The feedback and compensation loop configuration is discussed in the following sections.

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4.3. Gate Driving Circuit

SIC MOSFETs require higher gate-driving voltage than Si MOSFETs. A value of 20 V is recommended, as the device ON resistance will be lowest at this voltage. A reduced driving voltage will also work with a small increase in the R_{ds_on} value. The ON resistance increase is less significant at higher temperatures. **Figure 4** shows the ON resistance change with temperature at different gate driving voltages. Considering the maximum driving voltage limitation of the driver IC, 18 V driving is selected for this evaluation board. Compared with a 20 V driving voltage, 18 V driving will increase the ON resistance by 3.5% at 125 °C. A lower driving voltage can reduce short circuit peak current that might improve system ruggedness. However, if driving voltage is too low, the device may saturate at lower current and fail to support high peak current. Moreover, for overload conditions, the higher D-S voltage may not trigger the IC short circuit protection which would result in loss of protection during overload conditions.

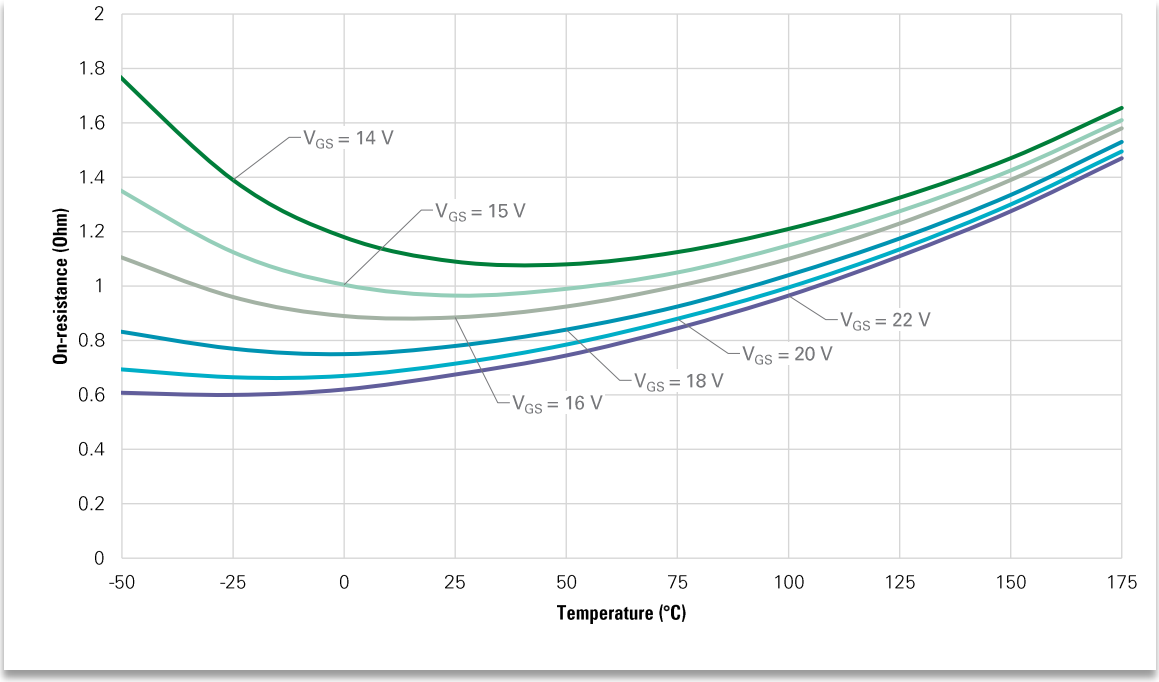

Figure 4. On-resistance vs. Temperature at Different Gate Driving Voltage

SiC MOSFETs have ultra-low input capacitance; therefore, the gate charge needed to turn on the devices is also very low. The PWM controller IC can drive power MOSFETs directly without the need for an additional driver IC, which can further reduce system costs. The selection of suitable gate resistance is a tradeoff between switching losses, switching speed, and EMI noise emission. A smaller gate resistance can increase power MOSFET switching speed and reduce switching loss; conversely, a larger gate resistance can reduce converter EMI noise emission. For SiC MOSFETs, turn on loss is usually higher than turn off loss with the same gate resistance. Therefore, different turn on and turn off resistances are recommended – a smaller turn on resistance for turn on loss reduction and a larger turn off resistance to reduce voltage ringing and EMI noise emission. Considering the internal gate resistance of SiC MOSFETs, the peak output current capability, and the output impedance of PWM controller, a turn on resistance of 10 ohms and a turn off resistance of 20 ohms is selected.

After the gate driving circuit scheme and parameters are determined, it is also very critical to optimize the actual layout of the gate loop. The key design target is to reduce the gate loop inductance and avoid near-field coupling to minimize gate ringing and avoid high peak gate voltage. The actual design layout used for this evaluation board is shown in section 5. PCB Layout.

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4.4. Control Power Supply Circuit and Active Start Up

As an off-line power supply source for industrial applications, the control power of the controller IC must be provided inside the converter. An auxiliary winding is needed from the transformer to provide the required power for the controller IC at steady state. Because the driver IC requires 18 V and the output voltage is 12 V, the auxiliary to secondary turns ratio of the transformer is selected at 5:3 and an 18 V Zener diode is selected to stabilize the auxiliary supply voltage to the controller IC.

During the startup of the circuit, there is no switching action from the MOSFET and no energy in the transformer windings. Therefore, start-up power will need to be drawn from the input DC link directly. A traditional solution is to use an RC network to provide the startup charge, but the resistor would dissipate continuous power during converter steady state operation, which will reduce the efficiency of the system. An active normal operation circuit is implemented to substitute the start-up RC and reduce this loss. During startup, the control power is provided through a 2 kV NPN Darlington transistor Q1 (Part number: STP03D200) and the resistor network from the input DC bus. When the input voltage is above the driver IC UVLO, the driver IC will generate a PWM signal and the transformer will start transferring power. Meanwhile, the reference 5 V voltage from the drive IC will turn on Q2 to pull down the basis of Q1 and turn off Q1, following which, power will be provided from the auxiliary winding of the transformer. Note that although part number STP03D200 provides a high gain at high blocking voltage, it also adds cost. Other options, such as part number STN0214, work in this design but at a reduced performance due to the lower gain and lower blocking voltage.

4.5. Transformer Design

The transformer is the key passive component in the design that ensures the proper operation of the whole converter. The core material and winding wire selection will determine the power loss and temperature rise of the transformer. The leakage inductance influences voltage ringing and peak voltage on the power MOSFET. It also determines the RCD clamping circuit design. The isolation capacitance influences the system Common Mode (CM) noise emission. **Table 2** lists the design specifications of the transformer.

Table 2. Transformer Design Specifications

Specifications	Value
Turns Ratio (Np-Ns, Pri:Sec)	36.3
Turns Ratio (Ns-Na, Sec:Aux)	3.5
Primary Side Inductance (L_P)	1.2 mH
Primary Side Peak Current (I_{P_MAX})	1.21 A
Primary Side RMS Current (I_{P_RMS})	0.46 A
Secondary Side RMS Current (I_{S_RMS})	5.58 A

Considering the 110 kHz switching frequency of the design, a PQ style of Ferrite material 3C97 from Ferroxcube (Part number PQ-2625-3C97) is selected as the magnetic core. From **Table 2**, a transformer design using 36 Turns for the primary, secondary 3 Turns, auxiliary 5 Turns is used. Keeping in mind the winding RMS current and core winding area, AWG# 28 coil winding copper wire for primary side and auxiliary side winding wire are used. To reduce winding AC loss at 110 kHz,10 strands of AWG#28 coil winding copper wire is parallel for secondary side winding. **Figure 5** shows two winding structures for different design targets.

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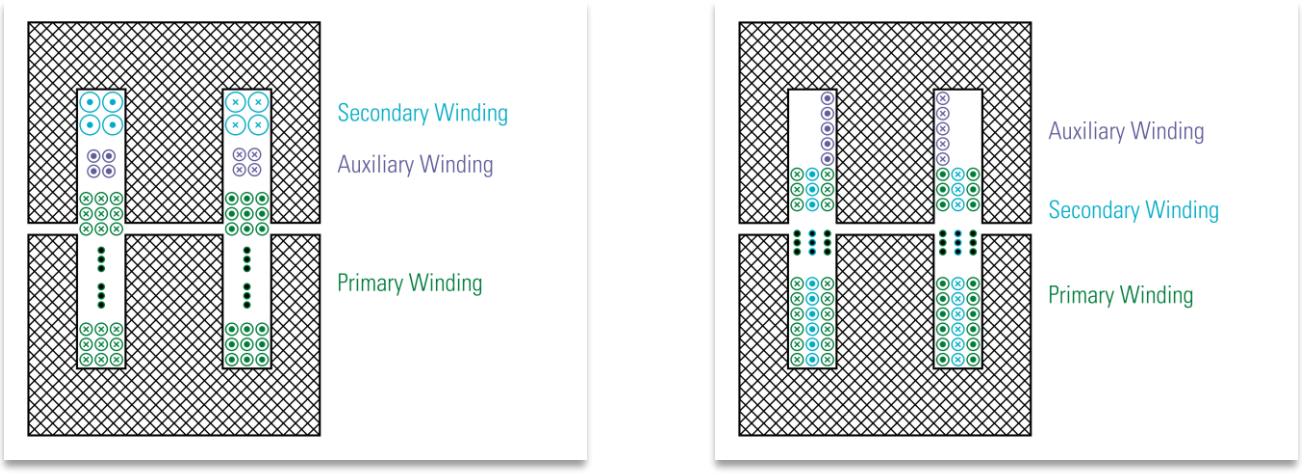


(a) Winding Structure for Good Isolation

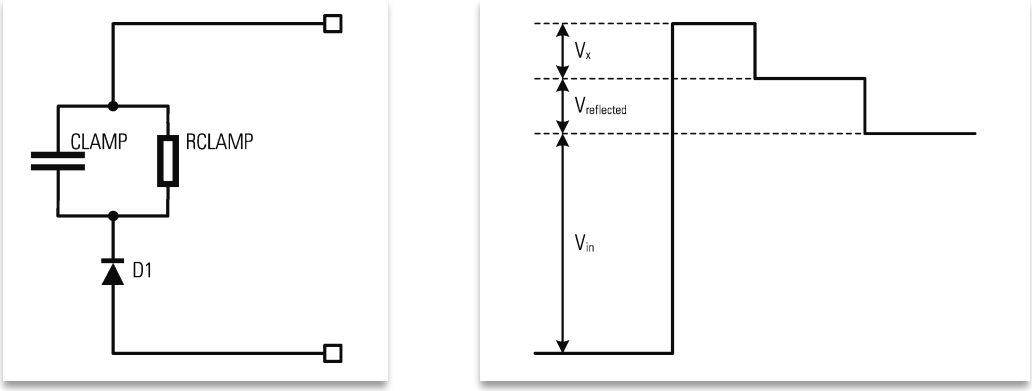
(b) Winding Structure for Low Leakage Inductance

Figure 5. Transformer Winding Structures

In **Figure 5 (a)**, the primary winding and secondary winding are separated to ensure good isolation between secondary winding and primary winding, which helps reduce the converter CM EMI emission. **Figure 5 (b)** interleaves the secondary winding and primary winding to minimize leakage inductance, which can help reduce the voltage ringing and clamping circuit power loss and improve system efficiency.

4.6. RCD Clamping

In fly-back topology, during the turn-off period, the primary side voltage rise charges any circuit capacitance, including the output capacitance of the MOSFET, in a relatively short time. When the primary voltage across the MOSFET exceeds the input voltage plus reflected output voltage, the secondary side diode conducts and the voltage across the transformer primary will be approximately clamped to the reflected output voltage. However, the turn-off of the MOSFET interrupts current through the leakage inductance of the transformer and this will cause a voltage spike on the MOSFET. The inductance will resonate with stray circuit capacitances and produce large-amplitude high-frequency ringing. This excessive voltage due to resonance should be suppressed to an acceptable level by an RCD clamping/snubber circuit. The RCD snubber circuit absorbs the energy from the leakage inductance resonance by forward biasing the diode when the device drain source voltage is higher than the input voltage plus the reflected output voltage. If the snubber capacitance is large enough, the voltage can be assumed constant during one switching period.



(a) RCD Clamping Circuit

(b) Simplified V_{ds} Waveform with RCD Clamping Circuit

Figure 6. RCD Clamping Circuit and Typical Waveform

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To design the snubber circuit, the leakage inductance of the transformer needs to be measured. We recommend using the leakage inductance measurement result at the switching frequency to estimate the energy stored in the leakage inductance, as shown in the following equation.

$$P_{leak} = \frac{1}{2} \times L_{leak} \times {I_{MOS\_max}}^2 \times f_s$$

The power dissipated by the RCD clamp components can then be calculated as:

$$P_{clamp} = P_{leak} \times \left(1 + \frac{V_{reflected}}{V_{in\_max}}\right)$$

SiC MOSFETs provide a higher margin of V_{max} and can therefore allow a lower snubber loss. The resistor value is critical in determining the peak voltage, as shown in the following equation:

$$R_{clamp} = \frac{\left(V_{reflected} + V_x\right)^2}{P_{clamp}}$$

In the equation above, $V_{reflected}$ is the voltage reflected from the secondary side and V_x is the voltage due to the energy stored in the snubber capacitor. The actual capacitance value is not critical in the snubber circuit design, but its value should be large enough to keep a small voltage ripple while absorbing the leakage energy. Considering 10% of the voltage ripple on the snubber capacitor, the capacitance can be calculated as:

$$C_{clamp} = \frac{1}{10\%} \times \frac{1}{R_{clamp} \times f_s}$$

4.7. Current Sensing Parameters

The current sensing circuits consist of the current sensing resistors R_{cs1}/R_{cs2} and filtering components R_8+C_{11}/C_{12}. The filtering components form a low pass filter that suppress the spikes in the sensing current due to the switching of SiC MOSFETs and reverse recovery of the output rectifier diode and parasitic effects in the power loop. The current sensing resistors R_{cs1}/R_{cs2} determine the maximum peak current in the primary side based on the maximum amplitude allowed in the driver IC, which is specified to be a minimum of 0.9 V. The upper limit of the sensing resistance is determined to ensure that cycle-by-cycle current limiting will not be triggered when the converter is operating at full power at minimum input voltage. Lower value sensing resistance reduces the sensing resistor losses. However, the sensing resistance should also be high enough to ensure the device current can be sensed over the whole range. In this design, a current sensing resistance of 0.65 ohm is selected and is implemented by two 1.3 ohm 2 W 1% 2512 SMD resistors in parallel.

4.8. Closed Loop Control Parameter

Closed loop control can eliminate steady state error and reduce the sensitivity of the system parametric change. Meanwhile, the gain and phase margin of the converter can be tailored over a certain frequency range to reduce the influence of small signal load disturbance and improve system load dynamic performance. Closed loop control has minimal influence on steady state performance. The drive IC is configured as a peak current mode PWM controller and an external voltage feedback loop is needed to stabilize the converter.

The design of the compensation loop includes three main parts: The TL431, the phototransistor optocoupler FOD817A and the error amplifier inside the controller IC. The voltage is sensed directly at the output after the output capacitors. A network of series resistors and capacitors is designed to set the pole/zero compensation location and the gain of the system. R_{23} and R_{24} set the output voltage on the TL431 to 12 V. R_{22}, C_{25} and C_{26} set the compensation zero location. R_{compp} and R_{fbg} set the DC gain of the error amplifier and C_{10} and R_{compp} set the compensation pole location. The control parameters of the voltage feedback loop need to consider the converter bode plot and determine the compensation parameters. This evaluation board is meant to demonstrate the power stage performance; therefore, precise RC value calculation for the voltage compensation loop design is not included in this application note [2].

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5. PCB Layout

Figure 7 and **Figure 8** show the PCB layout design of the evaluation board. A four-layer PCB configuration is selected for loop minimization purposes. Two main loops require to be minimized to ensure good performance of the power stage – one is the power loop in the primary side that includes the DC link and decoupling capacitors, SiC MOSFET, and the primary side of the transformer. A DC negative power plane covers most of the power circuit that ensures a low stray inductance and low EMI noise emission loop for the primary side. Another main loop to minimize is the gate driving loop which includes the SiC MOSFET gate, controller IC output pin, gate resistors, and gate driving loop decoupling capacitors. Minimizing the length of the driving loop and having a control ground plane under the gate driving signal propagation path to minimize the driving loop inductance and possible magnetic field coupling is recommended. Although the power ground plane and control ground plane have the same voltage potential, it is better to have separate physical power planes that have single grounding points in the actual implementation to avoid capacitive coupling between the power loop and gate loop.

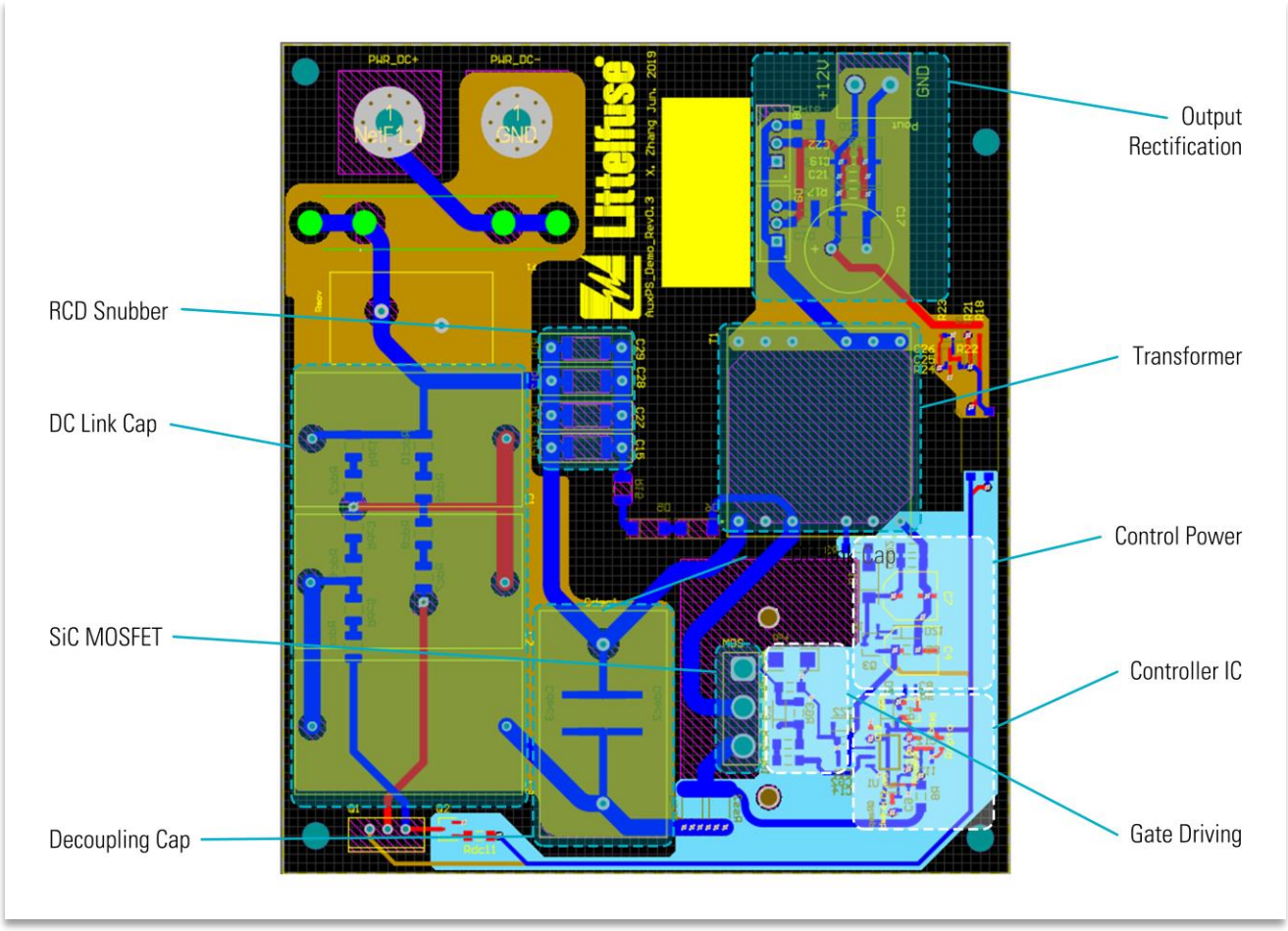

Figure 7. PCB Layout Design

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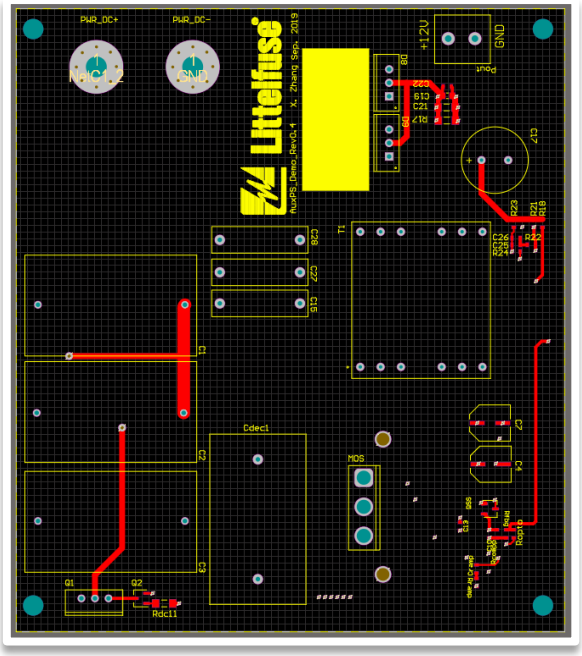
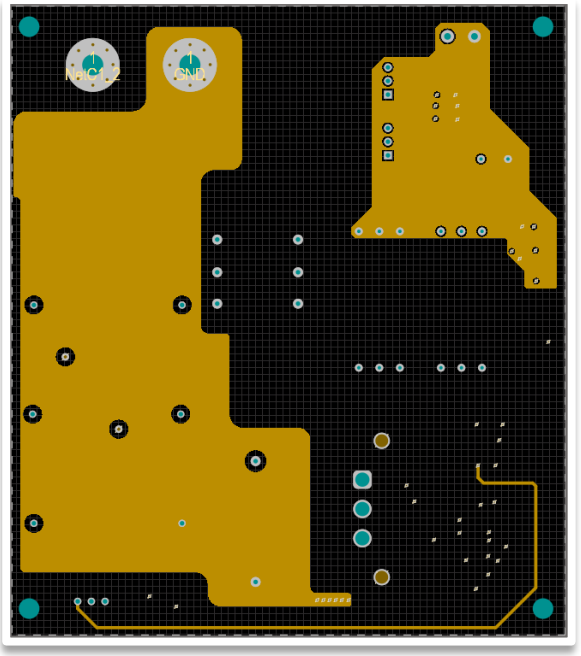
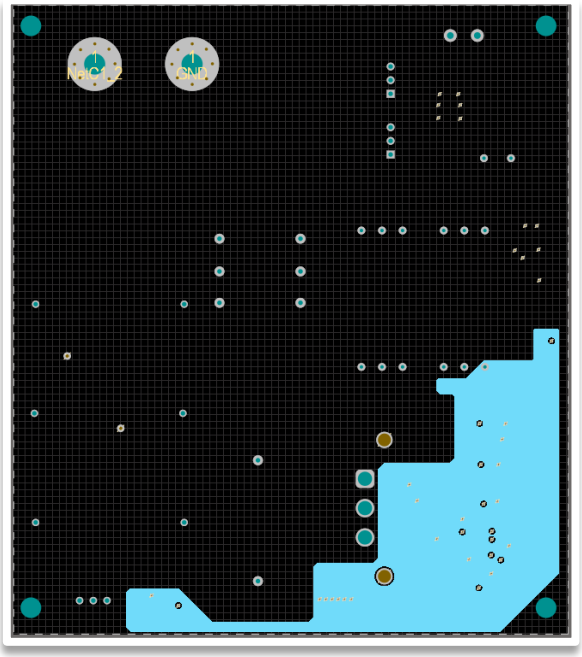


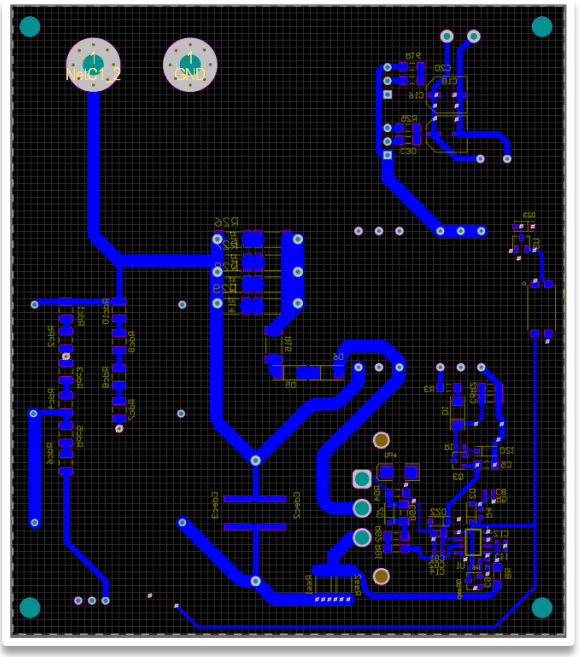
(a) Top Layer Copper and Top Side Component Placement



(b) Inner Layer 1 Copper



(c) Inner Layer 2 Copper



(d) Bottom Layer Copper and Bottom Side Component Placement

Figure 8. PCB Layout Design

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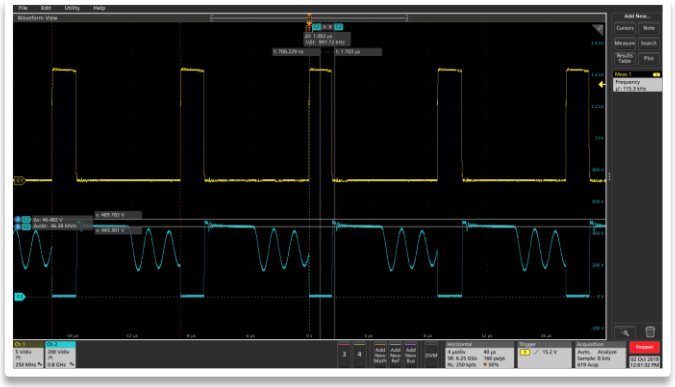
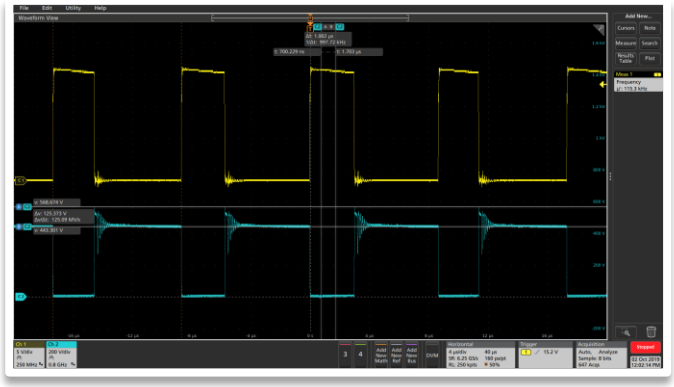
6. Test Results

6.1. Operation Waveforms

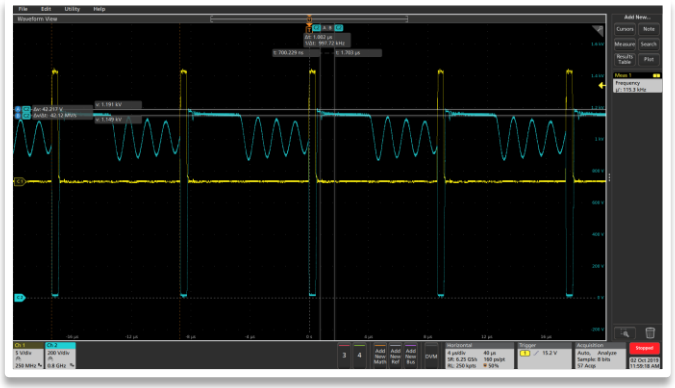
Figure 9 displays the SiC MOSFET drain to source voltage (V_{ds}) and gate to source voltage (V_{gs}) for different input voltages and different steady state output power levels. The converter works at CCM at full load and DCM at 20% load. The drain to source peak voltage on the MOSFET is 1265 V at 1000 V input voltage and full load condition. Device drain to source voltage is well clamped by the RCD circuit; however, there is still some V_{ds} ringing after device turn-off due to the relatively large leakage inductance of the transformer. The gate voltage has very small voltage overshoot and undershoot during device switching transient due to the relatively large gate resistance and good PCB layout design. The gate signal V_{gs} is very clean during the turn-on transient and there is little ringing during the turn-off transient due to V_{ds} ringing but the peak ringing voltage during turn-off is much lower than device threshold voltage. This SIC MOSFET device works well with 0 V gate voltage during turn-off.



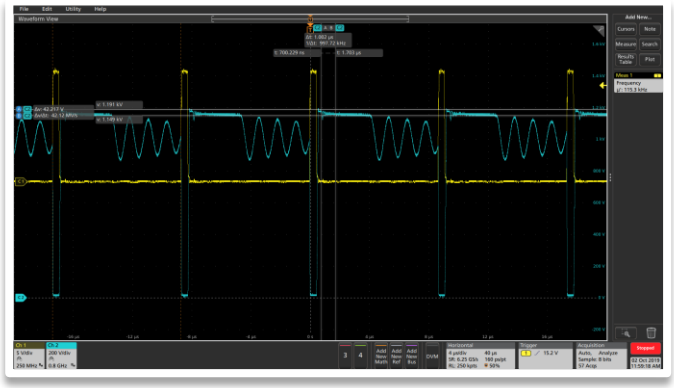
(a) V_{in} = 300 V, 20% Load (V_{gs}: Yellow; V_{ds}: Blue)



(b) V_{in} = 300 V, 100% Load (V_{gs}: Yellow; V_{ds}: Blue)



(c) V_{in} = 1000 V, 20% Load (V_{gs}: Yellow; V_{ds}: Blue)



(d) V_{in} = 1000 V, 100% Load (V_{gs}: Yellow; V_{ds}: Blue)

Figure 9. V_{ds} and V_{gs} at Different Input Voltage and Power Levels

6.2. Temperature Measurement

Figure 10 shows the thermal image measurement at full load under different input voltage conditions. There is no heatsink attached for the SiC MOSFET. A small heatsink is attached to the output diodes and the cooling condition is natural convection cooling. The results indicate that the SiC MOSFET maximum temperature reaches 106.5 °C at 1000 V input voltage and full load under room ambient temperature. This is the temperature performance without heatsink attached to the MOSFET; however, with a small heatsink, this temperature can be reduced. The output diode reaches 85 °C (thermocouple measurement on device top side) with a small heatsink attached. The transformer is less than 70 °C at full load and 1000 V input voltage. **Figure 11** shows the temperature rise

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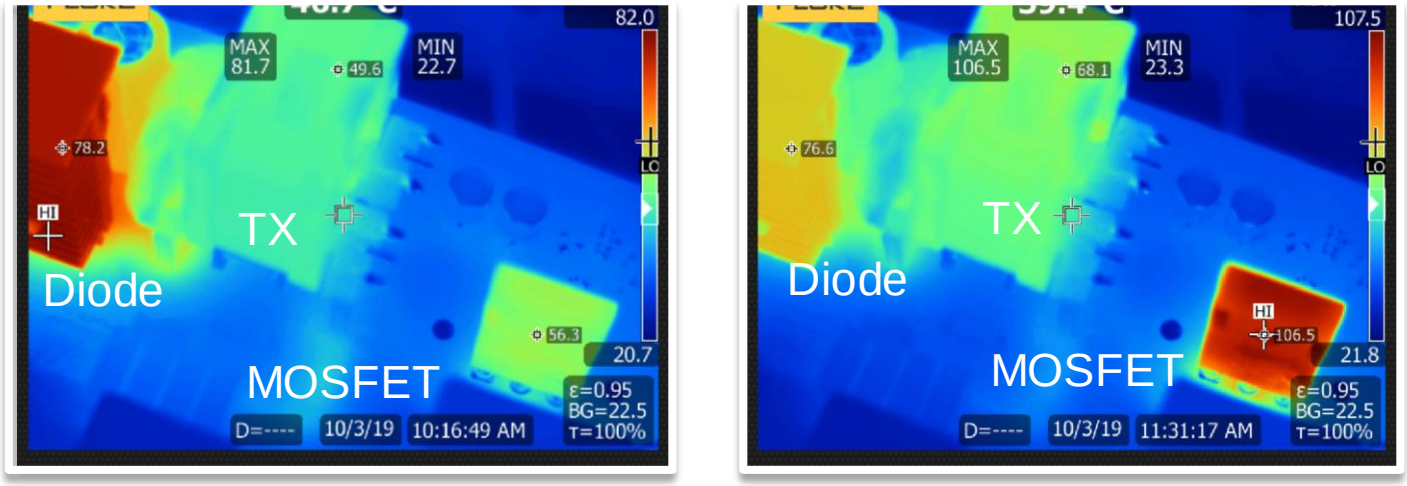
changes with input voltage at full load. The MOSFET temperature increases significantly when input voltage increases. This indicates that the MOSFET switching loss increases significantly when DC link voltage increase. Nonetheless, the temperature of transformer and output diode only increases slightly with input voltage.



(a) V_{in} = 300 V, 100% Load

(b) V_{in} = 1000 V, 100% Load

Figure 10. Thermal Image at Full Load under Different Input Voltage (Room Ambient Temperature)

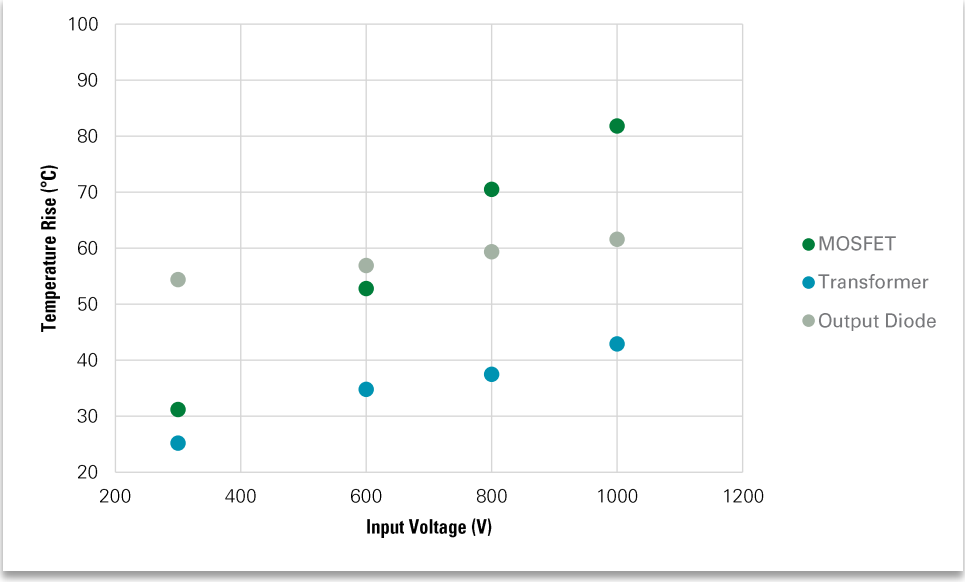


Figure 11. Temperature Rise at Full Load under Different Input Voltage

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6.3. Efficiency Measurement

Figure 12 displays the efficiency measurement results of the evaluation converter at various input voltage and load conditions. The converter efficiency is greater than 80% above 40% load for all input voltage conditions. A peak efficiency of 89.3% is achieved at 50% load and 300 V input voltage.

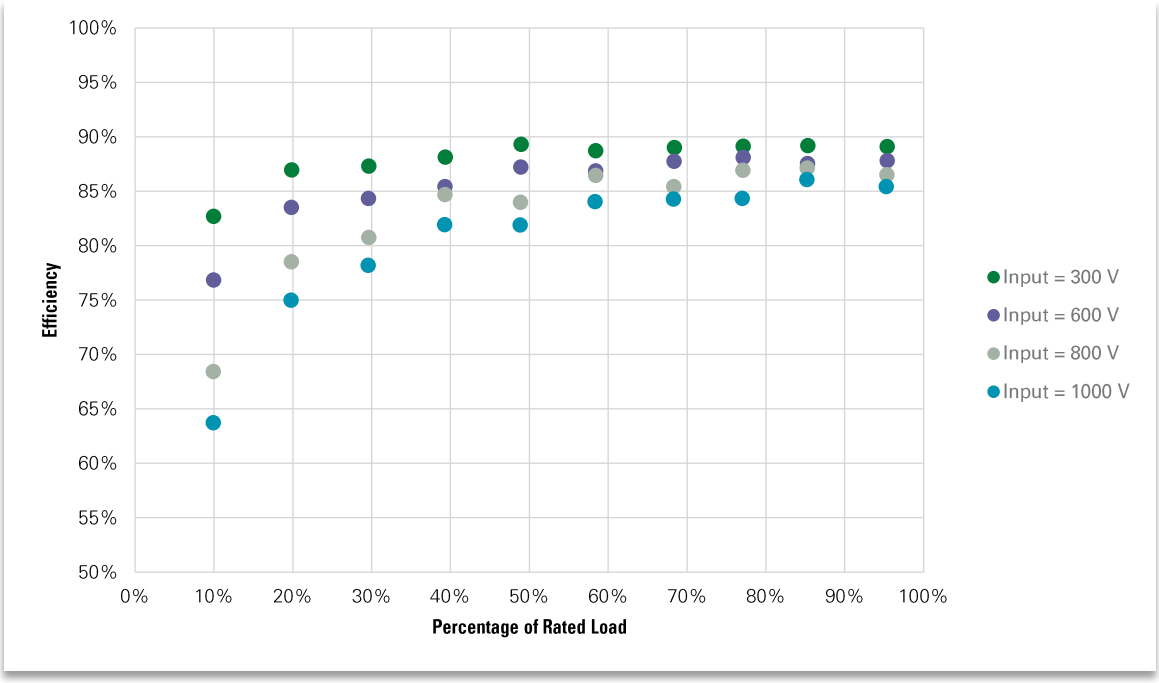

Figure 12. Measured Efficiency vs. Output Power under Different Input Voltage

7. Summary

This application note describes design details and presents the performance of a 60 W auxiliary power supply with wide input voltage for industrial applications using 1.7 kV 1 ohm SiC MOSFETs from Littelfuse. This document is intended for users of part number LSIC1MO170E0750 who wish to design low cost and high-performance off-line SMPS for auxiliary power supply. Various design details are discussed, including circuit parameter selection, PCB design layouts, and component implementations. Experimental test results including both electrical and thermal performances are presented. The design and testing results verify the advantage of using 1.7 kV SiC MOSFETs and demonstrate the benefit of simple structure, high efficiency, and low component count for a wide input range auxiliary power supply for industrial applications.

8. References

[1] Ray Ridley; Fly-back Converter Snubber Design; Switching Power Magazine; 2005

[2] Texas Instruments; UCCx8C4x BiCMOS Low-Power Current-Mode PWM Controller; Application Note; 2017

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