IXYS
INTEGRATED CIRCUITS DIVISION

IX4351NE
9A Low Side SiC MOSFET & IGBT Driver

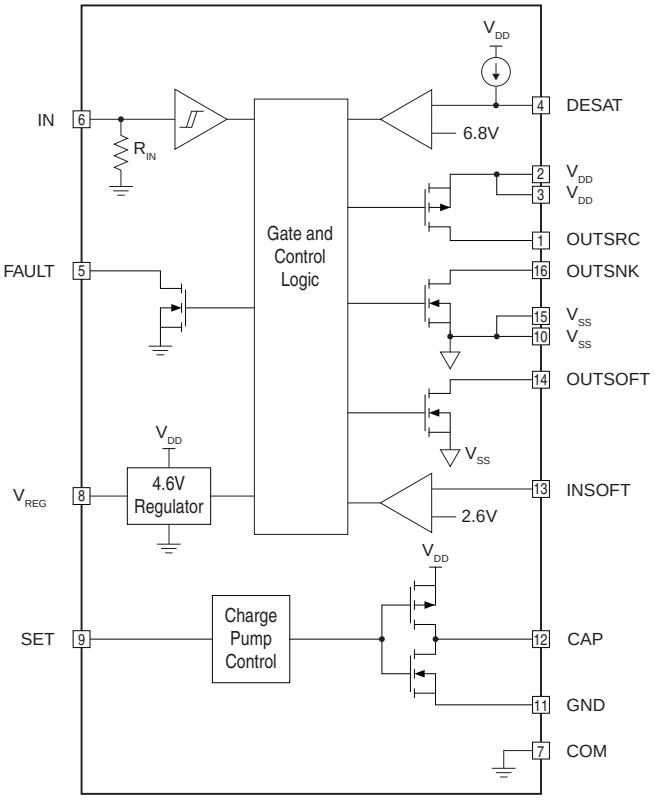
Features

- Separate 9A peak source and sink outputs
- Operating Voltage Range: -10V to +25V
- Internal charge pump regulator for selectable negative gate drive bias
- Desaturation detection with soft shutdown sink driver
- TTL and CMOS compatible input
- Under Voltage lockout (UVLO)
- Thermal shutdown
- Open drain FAULT output

Applications

- On-board chargers
- DC-DC converters
- Electric vehicle charging stations
- Motor controllers
- Power inverters

IX4351NE Functional Block Diagram



Description

The IX4351NE gate driver is designed specifically to drive SiC MOSFETs and high power IGBTs. Separate 9A source and sink outputs allow for tailored turn-on and turn-off timing while minimizing switching losses. An internal negative charge regulator provides a selectable negative gate drive bias for improved dV/dt immunity and faster turn-off.

Desaturation detection circuitry senses an over current condition of the SiC MOSFET and initiates a soft turn off, thus preventing a potentially damaging dV/dt event. The non-inverting logic input, IN, is TTL and CMOS compatible; internal level shifters provide the necessary bias to accommodate negative gate drive bias voltages. Additional protection features include UVLO detection and thermal shutdown. An open drain FAULT output signals a fault condition to the microcontroller.

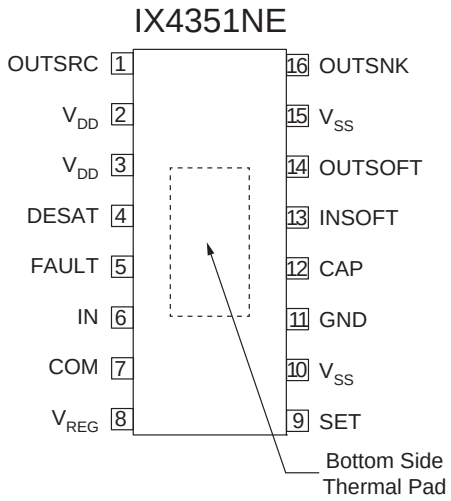
The IX4351NE is available in a thermally enhanced 16-pin narrow SOIC package.

Ordering Information

Part	Description
IX4351NE	16-Pin narrow SOIC with exposed thermal pad. In tubes (50/Tube)
IX4351NETR	16-Pin narrow SOIC with exposed thermal pad. In Tape & Reel (2000/Reel)

1 Specifications

1.1 Package Pinout



1.2 Pin Description

Pin#	Name	Pin Type	Description
1	OUTSRC	Output	Gate driver, source
2, 3	V_{DD}	Power	Positive supply voltage: Connect pin 2 to pin 3 on printed circuit board (PCB)
4	DESAT	Input	Sense input for desaturation detection
5	FAULT	Output	Fault status, Open-Drain, active low.
6	IN	Input	Logic input
7	COM	Power	Common ground connection: Connect to GND
8	V_{REG}	Output	4.6V regulator output
9	SET	Input	Sets negative supply voltage (V_{SS}) level
10, 15	V_{SS}	Power	Negative supply voltage: Connect pin 10 to pin 15 on the PCB
11	GND	Power	Charge pump ground connection: Connect to COM
12	CAP	Output	Charge pump output
13	INSOFT	Input	Soft Shutdown sense input
14	OUTSOFT	Output	Soft Shutdown - Gate driver, sink
16	OUTSNK	Output	Gate driver, sink
-	Thermal Pad	Thermal	Must be connected to V_{SS} or left floating. Do not connect to any other signal or net.

1.3 Absolute Maximum Ratings

Unless otherwise specified all voltages are with respect to V_{COM} and electrical ratings are over the operational ambient temperature range.

Parameter	Symbol	Minimum	Maximum	Units
Positive Supply Voltage	V_{DD}	-0.3	32	V
Negative Supply Voltage	V_{SS}	-10	0	V
Supply Voltage Range	V_{DD} - V_{SS}	-0.3	40	V
Ground Separation	V_{GND}	-0.3	+0.3	V
Gate Drive Output Voltages	V_{OUTSRC} , V_{OUTSNK} , $V_{OUTSOFT}$	V_{SS} - 0.3	V_{DD} + 0.3	V
Gate Drive Output Current	I_{OUTSRC} , I_{OUTSNK}	-	±9	A_P
IN Input Voltage	V_{IN}	-0.3	7	V
DESAT Input Voltage	V_{DESAT}	-0.3	V_{DD} + 0.3	V
SET Input Voltage	V_{SET}	- 1	7	V
FAULT Output Voltage	V_{FAULT}	-0.3	V_{DD} + 0.3	V
V_{REG} Output Voltage	V_{REG}	-0.3	7	V
Junction Temperature	T_J	-55	+150	°C
Storage Temperature	T_{STG}	-55	+150	°C

1.4 Recommended Operating Conditions

Parameter	Symbol	Minimum	Maximum	Units
Positive Supply Voltage	V_{DD}	13	25	V
Negative Supply Voltage	V_{SS}	-3.5	-10	V
Input Voltage	V_{IN}	0	5.5	V
Operating Ambient Temperature	T_A	-40	125	°C

1.5 Electrical Characteristics

Unless otherwise specified, electrical characteristics are guaranteed at: V_{DD}=20V, V_{SS}=-5V, COM=GND=0V, V_{INH}=5V, V_{INL}=0V, C_{DD}=C_{REG}=4.7µF, C_{SS}=10µF, and -40°C ≤ T_A ≤ +125°C.

1.5.1 V_{DD}

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Operating V_{DD} Supply Current	f_{IN}=100kHz, V_{SET}=0.4V, C_{LOAD}=2.2nF	I_{DD}	-	19	28	mA
Quiescent V_{DD} Supply Current	V_{IN}=0V, V_{SET}=-0.4V, No load	I_{DDQ}	-	2.9	4.4	mA
V_{DD} UVLO Rising Threshold	-	V_{DDUV+}	10	12	13	V
V_{DD} UVLO Hysteresis	-	V_{DDHYS}	-	2	-	V

1.5.2 V_{REG}

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Regulator Output Voltage	I_{REG}=-5mA	V_{REG}	4.2	4.6	5	V
Line Regulation	15V < V_{DD} < 25V, I_{REG}=-5mA	ΔV_{REG}	-	0.1	0.2	V
Load Regulation	-1mA ≤ I_{REG} ≤ -10mA		-	0.1	0.4	V

1.5.3 Charge Pump and V_{SS}

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Negative Supply Voltage Range	-	V_{SS}	-3.5	-	-8	V
Average V_{SS} Current	C_{FLY}=68nF, R_{FLY}=33Ω	I_{SS}	-	-	50	mA
Charge Pump Frequency	V_{SET} = -0.4V	f_{OSC}	90	124	160	kHz

1.5.4 Desaturation

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
DESAT Source Current	V_{DESAT}=0V	I_{DESAT}	400	570	750	µA
DESAT Detect Threshold Voltage	-	$V_{DESAT,TH}$	6	6.8	8	V
Blanking Time	C_{BLANK}=0µF	t_{BLANK}	-	250	-	ns
DESAT Pull Down On-Resistance	-	$R_{DST(on)}$	-	900	-	Ω

1.5.5 Thermal Shutdown

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Thermal Shutdown Temperature	-	TSD	-	160	-	°C
Thermal Shutdown Hysteresis	-	TSD_{HYS}	-	20	-	°C

1.5.6 IN

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
High Level Logic Input Voltage	-	V_{INH}	2.2	-	-	V
Low Level Logic Input Voltage	-	V_{INL}	-	-	1	V
Input Voltage Hysteresis	-	V_{INHYS}	0.2	0.4	-	V
High Level Input Current	V_{IN}=5V	I_{INH}	-	50	70	µA
Low Level Input Current	V_{IN}=0V	I_{INL}	-	-	-10	µA
Input Pull-Down Resistance	V_{IN}=5V	R_{IN}	-	100	-	kΩ

1.5.7 FAULT

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Output Low Voltage	I_{FAULT}=20mA	V_{FAULTL}	-	-	0.8	V
Output Leakage Current	V_{FAULT}=20V	I_{FAULT}	-	0.1	10	µA
DESAT Detect to FAULT Propagation Delay	-	$t_{FAULTDLY}$	-	150	-	ns

1.5.8 Soft Shutdown

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
Soft Shutdown Threshold Voltage	-	$V_{INSOFT,TH}$	2.3	2.6	3	V
Soft Shutdown Hysteresis	-	$V_{INSOFTHYS}$	-	0.4	-	V
OUTSOFT Peak Sink Current	-	$I_{OUTSOFT}$	-	900	-	mA
OUTSOFT On-Resistance	$I_{OUTSOFT}$=100mA	$R_{OUTSOFT}$	-	6	15	Ω
DESAT Detect to OUTSOFT Propagation Delay	-	$t_{OUTSOFTDLY}$	-	125	-	ns

1.5.9 Gate Drive Output

Parameter	Conditions	Symbol	Minimum	Typical	Maximum	Units
High Level Output Voltage	I_{OUTSRC}=-100mA	V_{OUTSRC}	V_{DD}- 0.25	-	-	V
Low Level Output Voltage	I_{OUTSNK}=100mA	V_{OUTSNK}	-	-	0.25	V
OUTSRC On-Resistance	I_{OUTSRC}=-100mA	R_{OUTSRC}	-	1.16	2	Ω
OUTSNK On-Resistance	I_{OUTSNK}=100mA	R_{OUTSNK}	-	0.8	1.5	Ω
Turn-On Propagation Delay Time	C_{LOAD}=1nF	t_{ON}	-	75	125	ns
Turn-Off Propagation Delay Time	C_{LOAD}=1nF	t_{OFF}	-	65	125	ns
Turn-On Rise Time	C_{LOAD}=1nF	t_R	-	10	20	ns
Turn-Off Fall Time	C_{LOAD}=1nF	t_F	-	10	20	ns

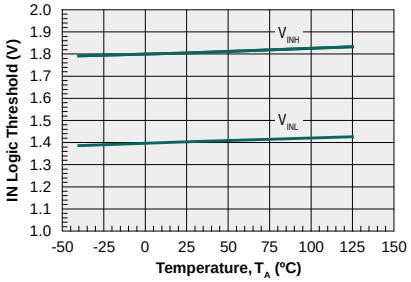
1.6 Thermal Characteristics

Parameter	Symbol	Rating	Units
Thermal Impedance, Junction to Ambient	θ_{JA}	60	°C/W
Thermal Impedance, Junction to Case	θ_{JC}	28	°C/W

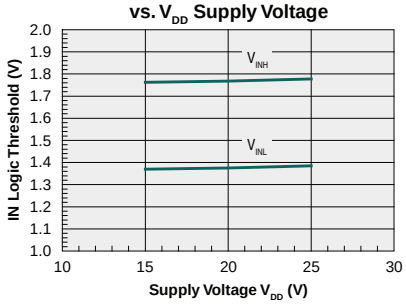
2 Performance Data

Unless otherwise noted V_{DD}=20V, T_A=25°C, and values are typical.

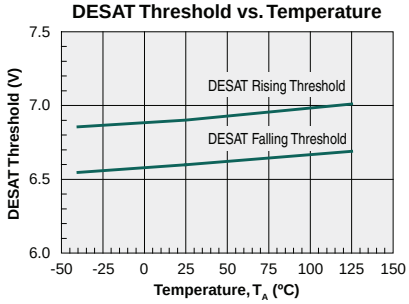
IN Logic Threshold vs. Temperature



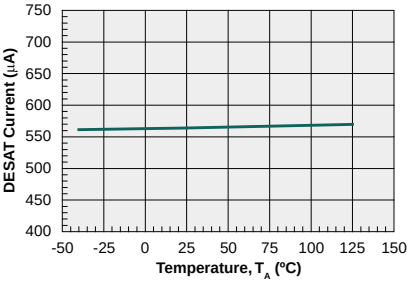
IN Logic Threshold vs. V_{DD} Supply Voltage



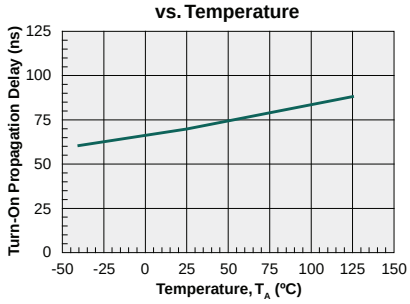
DESAT Threshold vs. Temperature



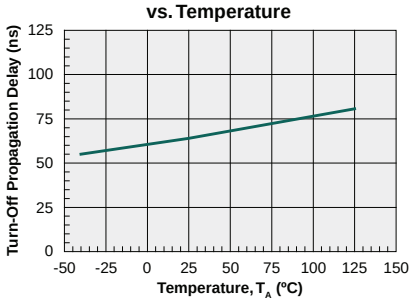
DESAT Current vs. Temperature



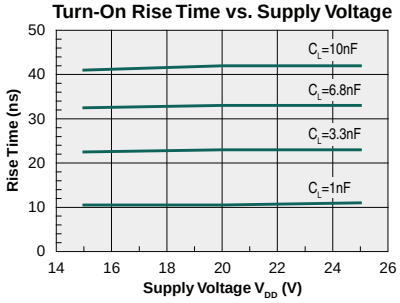
Turn-On Propagation Delay Time vs. Temperature



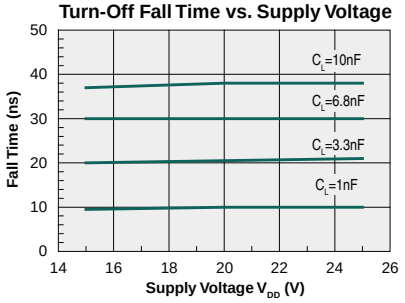
Turn-Off Propagation Delay Time vs. Temperature



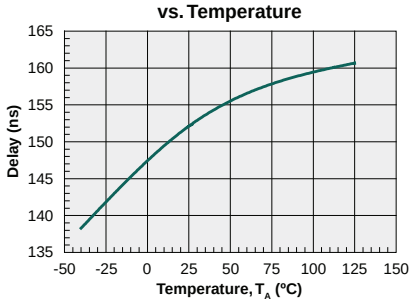
Turn-On Rise Time vs. Supply Voltage



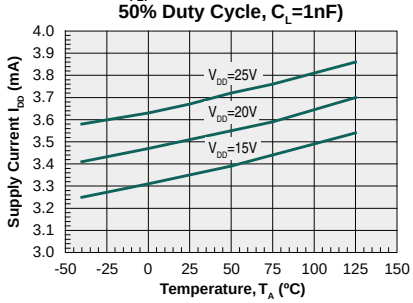
Turn-Off Fall Time vs. Supply Voltage



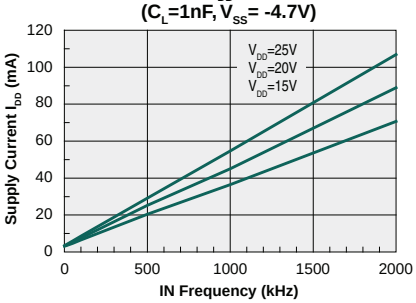
DESAT Detect to FAULT Delay vs. Temperature



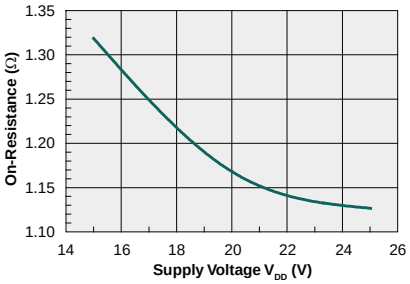
Supply Current I_{DD} vs. Temperature (C_{FLY}=68nF, IN: =1kHz, 0-5V, 50% Duty Cycle, C_L=1nF)



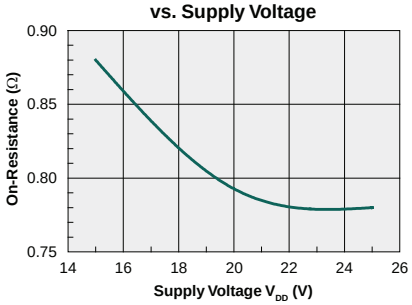
Supply Current I_{DD} vs. IN Frequency (C_L=1nF, V_{SS}= -4.7V)



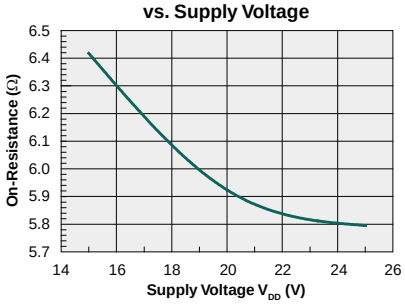
OUTSRC On-Resistance vs. Supply Voltage



OUTSNK On-Resistance vs. Supply Voltage



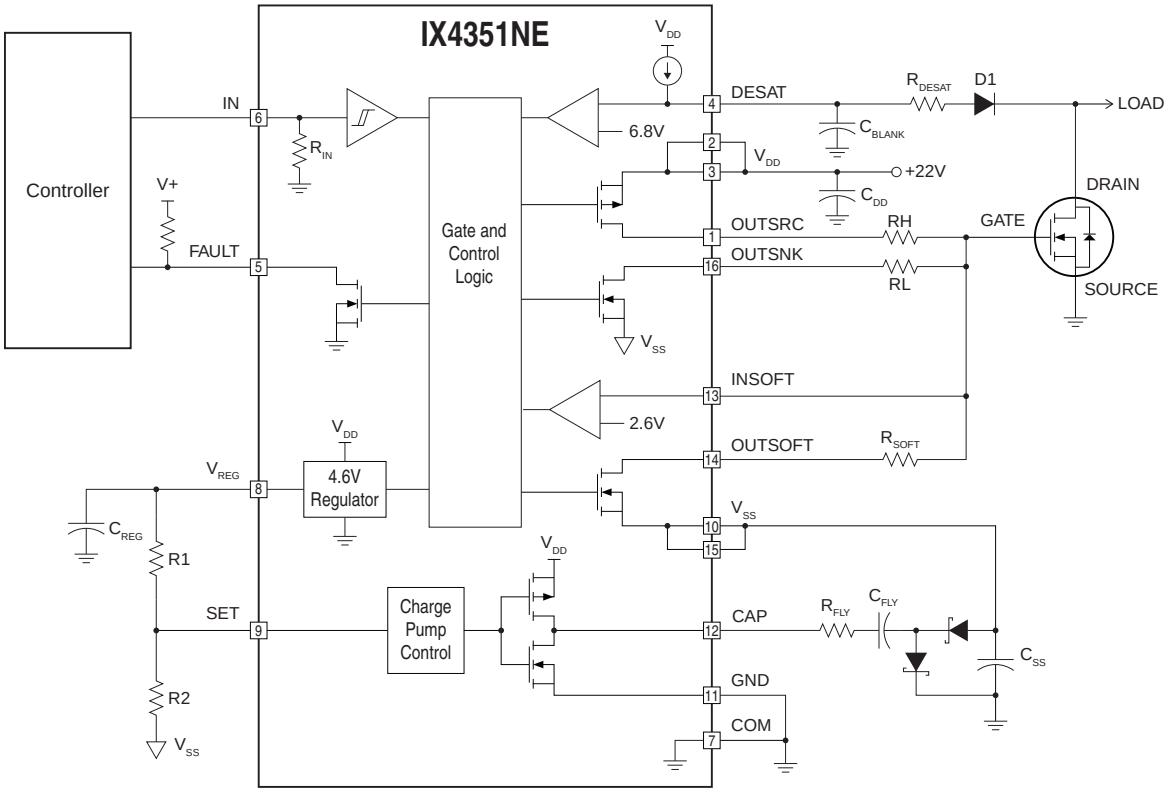
OUTSOFT On-Resistance vs. Supply Voltage



3 Functional Description

The IX4351NE is designed to provide the gate drive for high power SiC MOSFETs and IGBTs.

Figure 1. IX4351NE Typical Application Circuit



3.1 Power Supplies

The IX4351NE requires only a single positive supply (V_{DD}) to provide SiC and IGBT gate driver functionality by generating the negative voltage (V_{SS}) required to efficiently turn off SiC and IGBT power switches. V_{DD} provides the supply voltage for the gate driver outputs, the charge pump output driver and the internal low voltage regulator. An on-board regulator provides a low voltage supply (V_{REG}) used by the internal control logic while the on-board charge pump generates the pulses necessary to create the negative voltage supply (V_{SS}).

3.2 Logic Input (IN)

IN, the gate driver logic input, is a TTL and CMOS logic level compatible high-speed Schmitt trigger buffer that controls the gate driver outputs: OUTSRC, OUTSNK, and OUTSOFT. The input voltage logic thresholds have 0.4V of hysteresis and are referenced to COM. On startup, after V_{DD} and V_{SS} reach their minimum operating voltage levels by exceeding their Under Voltage Lock Out thresholds, IN controls the state of the gate driver outputs according to the table below:

Table 1: IN Gate Control Truth Table

IN	OUTSRC	OUTSNK	OUTSOFT
0	Off	Low	Low
1	High	Off	Off

3.3 Gate Drive Outputs

The IX4351NE has three gate drive outputs. Two power outputs, OUTSRC and OUTSNK, are rated for 9A peak current while the third output, OUTSOFT, is rated for 900mA peak current. Separate source and sink high current outputs allow independent adjustment of the discrete power SiC MOSFET or

IGBT turn-on and turn-off transactions by means of a single resistor for each output. An internal non-adjustable dead time prevents cross conduction of the source and sink outputs.

During normal operation whenever IN, the gate control input, is driven to a logic low the lower rated current sink output, OUTSOFT, turns on concurrently with OUTSNK. These operations can be seen in Figure 2, “Timing Diagram,” on page 11. In the timing diagram these normal operation transactions can be seen with the first cycle of the IN waveform.

3.4 Internal 4.6V Regulator (V_{REG})

The internal 4.6V regulator provides power for the internal low voltage control circuitry and requires an external 4.7µF bypass capacitor (C_{REG}). Capable of sourcing up to 10mA, V_{REG} is utilized to set the negative supply voltage level and optionally power the LED of an external optocoupler.

3.5 Negative Supply Voltage (V_{SS}) Generation

The IX4351NE inverting charge pump regulator circuitry outputs V_{SS}, a regulated negative supply voltage. Operating in a closed-loop mode the charge pump generates V_{SS} from V_{DD} with regulation being achieved by sensing the V_{SS} voltage with respect to V_{REG} at the SET input by means of the resistor divider R1 and R2. See Figure 1, “IX4351NE Typical Application Circuit,” on page 9 for the circuit configuration. The charge pump inverter requires two discrete Schottky diodes, two external ceramic capacitors, and a peak output current limiting resistor (R_{FLY}). V_{SS} is set by the R1 and R2 resistor divider given in the following equation:

$$V_{SS} = -V_{REG} \bullet \left(\frac{R2}{R1}\right) \quad \text{(Where R1 + R2 ~ 100k}\Omega\text{)}$$

The recommended value of the charge pump inverter components is:

1. R_{FLY} = 33Ω
2. C_{FLY} = 68nF
3. C_{SS} = 10uF

To prevent damaging the charge pump output, CAP, the value of R_{FLY} must not be reduced.

3.6 Desaturation Detection and Protection

DESAT detection occurs when the SiC or IGBT power transistor goes into an over-current condition causing the voltage across the transistor to exceed a predetermined threshold chosen by the designer.

The desaturation protection circuit ensures the safety of the external SiC MOSFET or IGBT during turn-off whenever the power switch is in an over-current situation. The DESAT pin monitors the drain voltage of the power SiC MOSFET or the collector of the power IGBT via the input circuitry between the DESAT input and the SiC MOSFET drain or the IGBT collector. When the sum of the drain or collector voltage plus the voltage drop of the DESAT input circuitry exceeds the DESAT Threshold Voltage ($V_{DESAT,TH}$), typically 6.8V, the FAULT output goes low, the internal MUTE function is activated and a controlled turn-off sequence is initiated. OUTSRC is turned off and OUTSOFT is turned on. The OUTSOFT 900mA sink capability provides an initial slow turn-off of the external SiC MOSFET or IGBT. When the GATE voltage decreases to the Soft Shutdown Threshold Voltage ($V_{INSOFT,TH}$), typically 2.6V, OUTSNK turns on and quickly pulls the GATE to V_{SS}. This two-step turn-off avoids dangerous dV/dt transient over-voltage spikes across the external SiC MOSFET or IGBT.

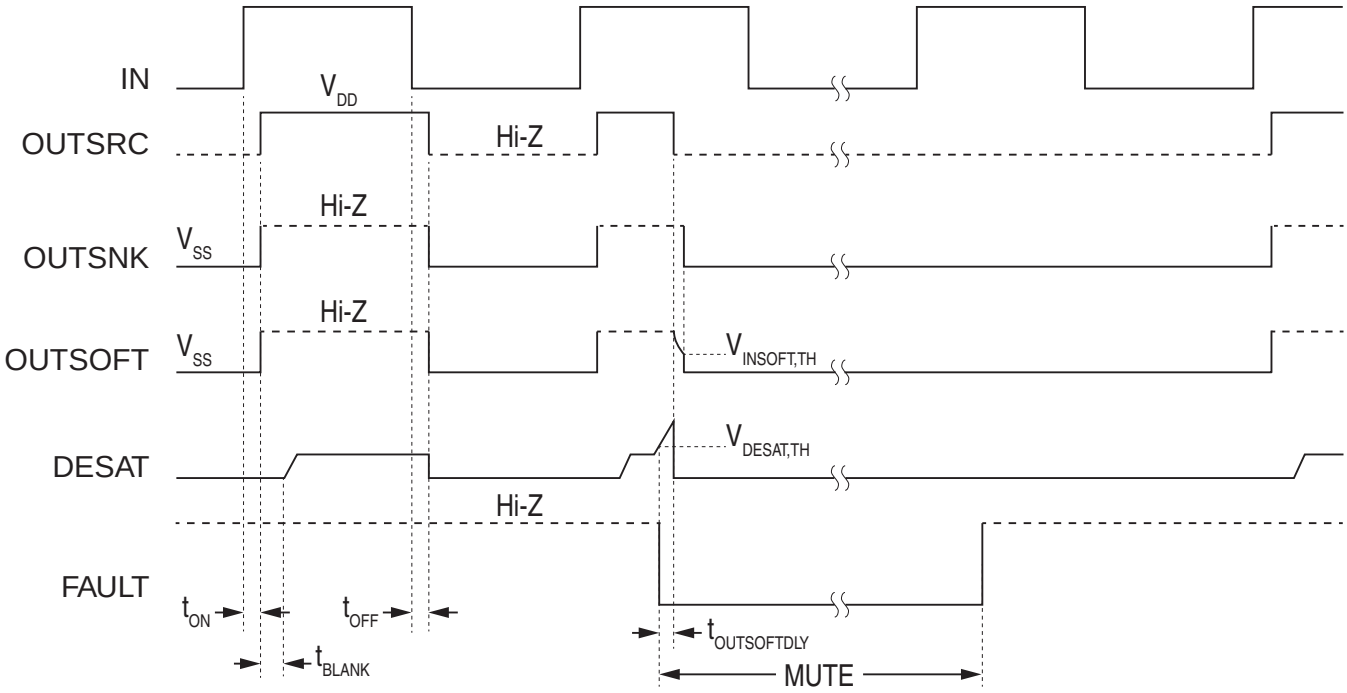
When DESAT is detected the MUTE feature is activated. MUTE holds FAULT low and masks logic inputs applied to IN for a nominal duration of 2ms. Once the MUTE timer expires, FAULT is released and the input will begin normal operation with the next low to high transition of IN.

The DESAT detection and two-step turn-off sequence can be seen in Figure 2, “Timing Diagram,” on page 11. In the timing diagram, this sequence begins with the second rising edge of IN.

To avoid a false desaturation detect event during turn-on of the external SiC MOSFET or IGBT, the IX4351 provides a nominal 250ns DESAT detect blanking time (t_{BLANK}) beginning when OUTSRC transitions from OFF to ON causing the gate drive output voltage to rise. While OUTSRC is off, the DESAT input is internally pulled low. To accomplish the fixed internal blanking time and to precondition the DESAT input for the fully turned on SiC MOSFET or IGBT, the DESAT input internal pull down remains active for the duration of the blanking period.

Although the nominal internal blanking duration is fixed at 250ns it can be extended by means of an external capacitor, C_{BLANK}, installed from the DESAT input to COM. Once the internal pull down is released, the additional blanking duration is set by the time it takes to charge the total external capacitive loading of the DESAT input up to $V_{DESAT,TH}$. The value of C_{BLANK} is the difference between the total capacitance required to obtain the desired blanking period less the capacitive loading of the other components on DESAT.

Figure 2. Timing Diagram



3.7 DESAT Input Component Selection

The value of R_{DESAT} is determined by the peak surge current permitted through diode D1 and the maximum voltage across the external power transistor. When IN is high and the power SiC MOSFET is on, the voltage at the DESAT input is calculated by the following equation.

$$V_{DESAT} = I_{DESAT} \cdot R_{DESAT} + V_f + V_{DS}$$

Substitute V_{CE} for V_{DS} when using an IGBT.

where V_f is the forward voltage drop of D1.

For a desired drain-to-source voltage ($V_{DS,TH}$), the desaturation detect threshold equation is:

$$V_{DESAT,\,TH} - V_{DS,\,TH} = I_{DESAT} \cdot R_{DESAT} + nV_f$$

Substitute $V_{CE,TH}$ for $V_{DS,TH}$ when using an IGBT.

where “n” is the number of series diodes in the DESAT detection input circuit.

Using multiple series diodes improves DESAT detection consistency by minimizing R_{DESAT}. Larger values of R_{DESAT} lessens DESAT detection uniformity due to variations of I_{DESAT}. This of course assumes the diode is operating above its forward bias knee voltage with a forward current of I_{DESAT}.

3.8 DESAT Blanking Time Stretching

Extending the blanking period is easily accomplished by the addition of an external capacitor to the DESAT input. Blanking time extension is the difference between the nominal 250ns fixed internal blanking period and the required total blanking time of the design.The equation for the total blanking time is given in the following equation.

$$t_{TOTAL} = 250ns + \frac{V_{DESAT,\,TH} \cdot C_{TOTAL}}{I_{DESAT}}$$

Where C_{TOTAL} is the total external capacitance seen by the DESAT input pin. For the design example shown in Figure 1, “IX4351NE Typical Application Circuit,” on page 9, C_{TOTAL} is the sum of C_{BLANK} and C_J, the junction capacitance of D1. C_{BLANK} is calculated as follows:

$$C_{BLANK} = \frac{(t_{TOTAL} - 250ns) \cdot I_{DESAT}}{V_{DESAT,\,TH}} - \frac{C_J}{n}$$

Where “n” is the number of series diodes in the DESAT detection input circuit.

Optionally the total capacitance may include the junction capacitance of a protection zener diode from DESAT to COM. Because this additional junction capacitance is added to C_{TOTAL} it reduces the calculated value of C_{BLANK}.

3.9 Thermal Shutdown

Thermal protection circuity pulls FAULT low, turns off OUTSRC, turns on both OUTSNK and OUTSOFT, and disables the charge pump whenever the IX4351NE internal junction temperature reaches a nominal +160°C. After the internal junction temperature decreases by approximately 20°C the device returns to normal operation.

3.10 FAULT Output

The FAULT output indicates the IX4351NE is undergoing a fault condition. The open-drain NMOS output pulls low whenever one of the four monitored fault conditions is detected. They are:

1. V_{DD} Under Voltage Lock Out.
   FAULT output goes low until V_{DD} UVLO clears.
   OUTSRC is turned off.
   OUTSNK and OUTSOFT go low.
   Charge pump disabled.
2. V_{SS} Under Voltage Lock Out.
   FAULT output goes low until V_{SS} UVLO clears.
   OUTSRC is turned off.
   OUTSNK and OUTSOFT go low.
   Charge pump continues running.
3. DESAT detection.
   FAULT output goes low for a nominal 2ms.
   OUTSRC is turned off.
   OUTSOFT goes low.
   Gate voltage crosses $V_{INSOFT,TH}$
   OUTSNK goes low.
   Charge pump unaffected.
4. Thermal Shut Down.
   FAULT output goes low until TSD clears.
   OUTSRC is turned off.
   OUTSNK and OUTSOFT go low.
   Charge pump disabled.

When the UVLO and TSD faults clear, the IX4351NE returns to normal operation and the gate driver outputs immediately transition to comply with the current IN logic state.

When the DESAT fault clears, the FAULT output remains low until the 2ms MUTE timer expires. The gate drive outputs remain low until the next low to high IN transition after the MUTE timer expires.

4 Manufacturing Information

4.1 Moisture Sensitivity

All plastic encapsulated semiconductor packages are susceptible to moisture ingression. IXYS Integrated Circuits classifies its plastic encapsulated devices for moisture sensitivity according to the latest version of the joint industry standard, **IPC/JEDEC J-STD-020**, in force at the time of product evaluation. We test all of our products to the maximum conditions set forth in the standard, and guarantee proper operation of our devices when handled according to the limitations and information in that standard as well as to any limitations set forth in the information or standards referenced below.

Failure to adhere to the warnings or limitations as established by the listed specifications could result in reduced product performance, reduction of operable life, and/or reduction of overall reliability.

This product carries a **Moisture Sensitivity Level (MSL)** classification as shown below, and should be handled according to the requirements of the latest version of the joint industry standard **IPC/JEDEC J-STD-033**.

Device	Moisture Sensitivity Level (MSL) Classification
IX4351NE	MSL 1

4.2 ESD Sensitivity

This product is **ESD Sensitive**, and should be handled according to the industry standard **JESD-625**.

4.3 Soldering Profile

Provided in the table below is the **IPC/JEDEC J-STD-020** Classification Temperature (T_C) and the maximum dwell time the body temperature of these surface mount devices may be (T_C - 5)°C or greater. The Classification Temperature sets the Maximum Body Temperature allowed for these devices during reflow soldering processes.

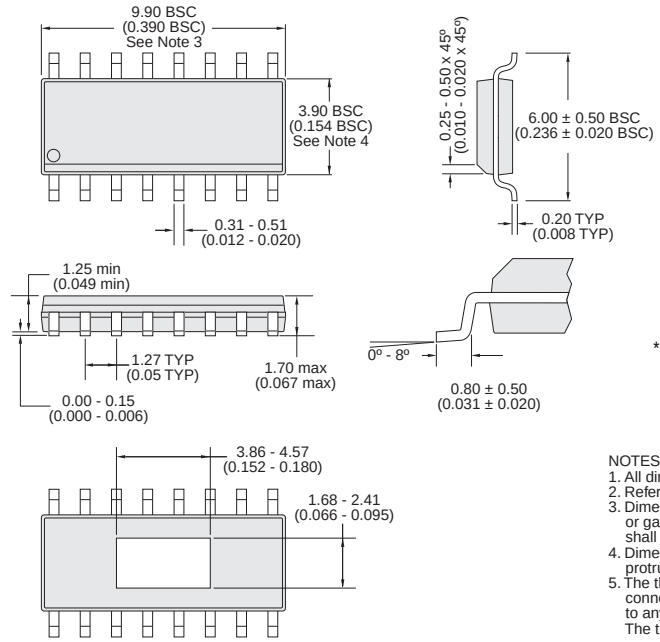
Device	Classification Temperature (T_C)	Dwell Time (t_p)	Max Reflow Cycles
IX4351NE	260°C	30 seconds	3

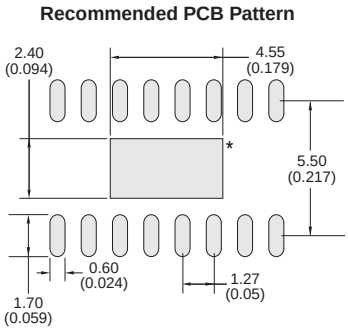
4.4 Board Wash

IXYS Integrated Circuits recommends the use of no-clean flux formulations. Board washing to reduce or remove flux residue following the solder reflow process is acceptable provided proper precautions are taken to prevent damage to the device. These precautions include but are not limited to: using a low pressure wash and providing a follow up bake cycle sufficient to remove any moisture trapped within the device due to the washing process. Due to the variability of the wash parameters used to clean the board, determination of the bake temperature and duration necessary to remove the moisture trapped within the package is the responsibility of the user (assembler). Cleaning or drying methods that employ ultrasonic energy may damage the device and should not be used. Additionally, the device must not be exposed to halide flux or solvents.

4.5 Mechanical Dimensions

4.5.1 IX4351NE 16-Pin Narrow SOIC Package



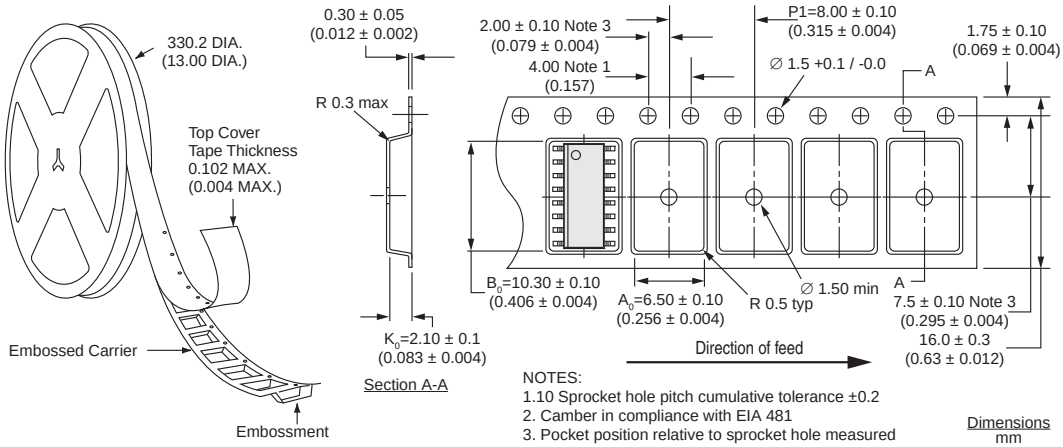


* Connect thermal pad to V_{SS} or leave open.

DIMENSIONS
mm
(inches)

NOTES:
1. All dimensions are MM (IN)
2. Reference JEDEC outline: MS-012 BC Rev F. (Thermal)
3. Dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, and gate burrs shall not exceed 0.15 (0.006) per side.
4. Dimension does not include inter-lead flash, and protrusions shall not exceed 0.25 (0.010) per side.
5. The thermal pad on the bottom of the device may be connected to V_{SS} or left floating; it must not be connected to any other signal.
   The thermal pad is not intended to carry current.

4.5.2 IX4351NETR Tape & Reel Packaging for 16-Pin Narrow SOIC Package



NOTES:
1.10 Sprocket hole pitch cumulative tolerance ±0.2
2. Camber in compliance with EIA 481
3. Pocket position relative to sprocket hole measured as true position of pocket, not pocket hole

Dimensions
mm
(inches)

For additional information please visit our website at: https://www.ixysic.com

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