

FPU-16

MODBUS PROTOCOL/DATA LOGGER MANUAL

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PRELIMINARY

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FPU-16 MODBUS PROTOCOL

1. MODBUS PROTOCOL DESCRIPTION

The FPU-16 implements the Modbus RTU protocol as described in the Gould Modbus Reference Guide, Publication PI-MBUS-300 Rev. B.

The communication system consists of a single master and up to 62 FPU-16 slaves. All devices are connected using two-wire RS-485 network hardware. If the master does not have an RS-485 port, a RS-232 to RS-485 converter is required. The converter must have automatic send-data control (SD). SD control does not require hand-shaking lines since it uses the data line to control the transmit/receive line on the RS-485 transceivers.

Only the master can initiate a message transaction. Messages can be addressed to individual slaves or they can be broadcast messages. Broadcast messages are executed on the FPU-16 slaves but unlike individually addressed messages, the slaves do not generate a reply message.

2. MODBUS MESSAGE SYNCHRONISATION

Message synchronisation is accomplished by detection of an idle communication line. The communication line is considered idle when no communication exists for an equivalent delay of 3.5 characters.

The first byte received after idle-line detection is interpreted as the address byte of the next message. Message bytes must be transmitted in a continuous stream until the complete message has been sent. If a delay of more than 3.5 characters exists within the message, the message is discarded.

Response messages from the FPU-16 are delayed by at least 3.5 character delays.

3. ERROR CHECKING

Modbus RTU uses a 16-bit cyclic redundancy check (CRC). The error check includes all of the message bytes, starting with the first address byte.

The following procedure generates the CRC for a message:

```
CONSTANT = A001 (HEX)
CRC_REGISTER = FFFF (HEX)

FOR each data_byte in the message:
    GET data_byte
    XOR (data_byte, right 8 bits of CRC_REGISTER)
    DO 8 times
        SHIFT CRC_REGISTER 1 bit to the right
        IF bit shifted out was a 1
            XOR (CONSTANT, CRC_REGISTER)
        END IF
    END DO
END FOR
```

The contents of the CRC_REGISTER is appended to the message with the LSB first, followed by the MSB.

When a CRC error is detected in the FPU-16, the message is discarded and there will be no response from the FPU-16.

If the CRC check is correct but the internal data in the message is not correct, the FPU-16 will respond with one of two exception responses listed in Section 4.4.

4. COMMANDS SUPPORTED

The FPU-16 Modbus Protocol supports three command messages, Read Coils, Read Output Registers, and Preset Single Register.

In the Modbus Protocol, holding registers are accessed using function code 03 and 06, and start at 40001 decimal. For example, the first holding register in a 584 would be register 40001 and the output register address generated for the message would be 0000.

Coils are accessed using function code 1 and are numbered from zero (coil 1 = zero, coil 2 = one, etc.).

All FPU-16 data can be accessed using the holding register command codes 03 and 06. Alternately, the holding registers can also be read as 16 bits using the coil-read command code 01.

4.1 READ REGISTERS AS COILS (CODE 01)

Each of the 16 bit registers in the FPU-16 can be read as groups of 16 bits or coils using this command.

The first byte of the message is the slave address. The second byte is the function code (01). Bytes three and four specify the starting coil address and the next two bytes specify the number of coils to read. The last two bytes contain the CRC code for the message.

The two-byte values of starting coil address and number of coils to read are transmitted with the high-order byte followed by the low-order byte.

To read a holding register as 16 coils, you specify the starting register number as the starting coil and request 16 coils.

For example, to read the trip status of holding register 40041 in slave #10 as 16 coils, you specify the starting address as 41 and request 16 coils (coils 41 to 56). The FPU-16 responds by sending two bytes of information. These two bytes are interpreted as 2 groups of 8 coils for a total of 16 coils.

READ COILS	
HEX BYTE	DESCRIPTION
0A	Slave Address
01	Function Code
00	MSB of First Coil Address
28	LSB of First Coil Address
00	MSB of Number of Coils
10	LSB of Number of Coils
BC	LSB of CRC
B5	MSB of CRC

FIGURE 1

Coils must read in groups of 16 and the starting coil address must be the same as the register address (except the coils start at 0001 instead of 40001).

4.2 READ OUTPUT REGISTERS (CODE 03)

Read Output Registers allows the user to obtain information from the FPU-16 in 16-bit format.

The first byte of the message is the slave address,. The second byte is the function code (03). Bytes three and four indicate the starting register. The next two bytes specify the number of 16-bit registers to read. The last two bytes contain the CRC code for the message.

The two-byte values of starting register and number of registers to read are transmitted with the high-order byte followed by the low-order byte.

The CRC value as calculated in Section 3 is sent with the LSB first followed by the MSB.

The following message will obtain the value of register 2 (Modbus 40002) from slave 1. Note that the Modbus registers are numbered from zero (40001 = zero, 40002 = one, etc.).

READ OUTPUT REGISTERS	
HEX BYTE	DESCRIPTION
01	Slave Address
03	Function Code
00	MSB Register Address
01	LSB Register Address
00	MSB Number of Registers
01	LSB Number of Registers
D5	LSB CRC
CA	MSB CRC

FIGURE 2

The message length for this message is fixed at 8 bytes.

The addressed slave responds with its address and function code (03), followed by the information field. The information field contains an 8-bit byte count and the 16-bit data from the slave. The byte count specifies the number of bytes of data in the information field. The data in the information field consists of 16-bit data arranged so that the MSB is followed by the LSB.

4.3 WRITE TO REGISTER

Function code 06 or 16 is used to make set-point changes. The FPU-16 does not allow setting multiple registers so when using function code 16, only one register should be set.

4.3.1 MESSAGE FORMAT FOR FUNCTION CODE 06

The message to the FPU-16 consists of the FPU-16 address followed by the function code 06 and two 16-bit values. The first 16-bit value specifies the internal FPU-16 register to be modified and the second value is the 16-bit data.

Provided no errors occurred, the slave will re-send the original message to the master. The response message is returned only after the command has been executed on the FPU-16. This will take approximately 300 ms.

The following message will set register 4 to 300 in slave #5.

PRESET SINGLE REGISTER USING CODE 06

HEX BYTE	DESCRIPTION
05	Slave Address
06	Function Code
00	MSB Register Address
03	LSB Register Address
01	MSB of Data
2C	LSB of Data
78	LSB of CRC
03	MSB of CRC

FIGURE 3

4.3.2 MESSAGE FORMAT FOR FUNCTION CODE 16

The FPU-16 supports pre-setting a single register using function code 16. Pre-setting multiple registers is not supported.

Figure 4 shows the message for setting register 4 to 300 in slave #5.

PRESET SINGLE REGISTER USING CODE 16

HEX BYTE	DESCRIPTION
05	Slave Address
10	Function Code
00	MSB Register Address
03	LSB Register Address
00	MSB of Quantity (Must be 00)
01	LSB of Quantity (Must be 01)
02	Byte Count (Must be 02)
01	MSB of Data
2C	LSB of Data
94	LSB CRC
EE	MSB CRC

FIGURE 4

The FPU-16 will reply with the Slave Address, Function Code, Register Address, and the Quantity followed by the CRC Code for a total of 8 bytes.

4.4 EXCEPTION RESPONSES

The FPU-16 supports two exception responses, Illegal Address and FPU Busy.

The exception message consists of the slave address followed by a retransmission of the original function code. The function code will have the most-significant bit set to indicate on error. The 8-bit byte following the function code is the exception response code. The 16-bit CRC is at the end of the message.

4.4.1 ILLEGAL ADDRESS (CODE 2)

This error indicates that the register number specified in the data field of the master message is not an allowable register address for the FPU-16.

4.4.2 FPU BUSY (CODE 6)

This error occurs when a valid message was received but the FPU-16 was busy processing a long duration program command. The message must be retransmitted at some later time.

5. FPU-SPECIFIC INFORMATION

The FPU-16 serial-port data base is updated every 300 ms. Database values can be read one by one or as a group. Since these values are updated every 300 ms, the master need not read these values any faster than 300 ms. In the case of set point-write or reset commands, only one set point or reset command may be processed every 300 ms.

Unused registers (0x12 to 0x17) must not be included in read/write instructions. If all information must be retrieved, two instructions are required. One instruction is used for set-point memory and the other is used for display memory.

5.1 DATA BASE

5.1.1 SET POINT MEMORY

You can read or write to the set-point memory. Individual or groups of set points can be read; however, set points must be written one at a time and only one set point may be changed every 300 ms.

Set-point memory is organised in 16 bit words. Data-base values less than 256 will have 0 stored in the high-order byte. Data-base values are transmitted as two 8-bit bytes, with the high byte transmitted first.

Set-point write instructions must have the data in the 16-bit format. Set-point values greater than the delete value are forced to the appropriate delete value. For set points with no delete value, the maximum value of the range is stored. Set-point values below the minimum are forced to the minimum value.

SET POINT MEMORY

MODBUS NO.	REG. NO.	SET POINT (16 BIT)	RANGE	DELETE	INCREMENT
40001	0x00	I ² t Trip	1-45	46	1
40002	0x01	I ² t Alarm	1-45	46	1
40003	0x02	Short Time Trip ⁽¹⁾	10-90	91	1
40004	0x03	Short-Time Alarm ⁽¹⁾	10-90	91	1
40005	0x04	Instantaneous Trip ⁽¹⁾	10-90	91	1
40006	0x05	Instantaneous Alarm ⁽¹⁾	10-90	91	1
40007	0x06	Unbalance Trip	5-75	76	1
40008	0x07	Unbalance Alarm	5-75	76	1
40009	0x08				
40010	0x09				
40011	0x0A	Earth-Leakage Trip	1-100	101	1
40012	0x0B	Earth-Leakage Alarm	1-100	101	1
40013	0x0C	FLA	(.45-.93)*CT-Primary Rating		
40014	0x0D				
40015	0x0E	Mode 5 Level 1	0-255		1
40016	0x0F	Mode 5 Level 2	0-255		1
40017	0x10	CT-Primary Rating	20-1200		5
40018	0x11	EFCT-Primary Rating	5, 50-2000		50

⁽¹⁾ Set point is 10 times actual value. A value of 15 corresponds to 1.5 X Phase-CT-Primary Rating.

TABLE 1

The high-order nibble of Mode 8 level 2 contains the FPU station address. This value cannot be changed via the serial port.

5.1.2 DISPLAY MEMORY

Display memory is read-only memory organised in 16 bit words. Display values less than 256 will have 0 stored in the high-order byte. Data-base values are transmitted as two 8-bit bytes, with the high byte transmitted first.

DISPLAY MEMORY

MODBUS NO.	REG. NO.	DESCRIPTION
40025	0x18	Phase A Current
40026	0x19	Phase B Current
40027	0x1A	Phase C Current
40028	0x1B	Unbalance
40029	0x1C	Earth Leakage ⁽¹⁾
40030	0x1D	Percent I ² t
40031	0x1E	Pre-Trip Phase A
40032	0x1F	Pre-Trip Phase B
40033	0x20	Pre-Trip Phase C
40034	0x21	Pre-Trip Unbalance
40035	0x22	Pre-Trip Earth Leakage ⁽¹⁾
40036	0x23	Pre-Trip I ² t
40037	0x24	Operation Count
40038	0x25	Reset Time
40039	0x26	Spare
40040	0x27	Station Address of FPU
40041	0x28	Trip Status Bits
40042	0x29	Alarm Status Bits
40043	0x2A	Motor Status Bits

⁽¹⁾ Divide reading by 10 for actual amperes.
 Resolution 1/10 A.

TABLE 2

5.1.3 RESET MEMORY

The memory location 0x0078 (40121) is reserved for the reset function and is a write-only location. The 16-bit data specifies the reset function. A write to register 0x0078 (40121) will perform the function indicated. Only one reset function is processed every 300 ms.

RESET MEMORY

DATA	DESCRIPTION
0000	Null Function ⁽²⁾
0001	Trip Reset
0002	Latches-Alarm Reset
0003	Not Used
0004	Emergency Thermal Reset
0005	Not Used
0006	FbAd Reset

⁽²⁾ This function accesses the FPU-16 processor but does not perform any function.

TABLE 3

5.1.4 TRIP-STATUS-BIT DEFINITIONS

The trip status bits indicate the FPU-16 trip conditions.

TRIP STATUS BITS	
BIT NUMBER	TRIP FUNCTION
0 (LSB)	1 = I ² t Trip
1	1 = Short-Time Trip
2	1 = Instantaneous Trip
3	1 = Unbalance Trip
4	1 = Earth-fault Trip
5	Not Used
6	Not Used
7	1 = Memory-Fault Trip

TABLE 4

5.1.5 ALARM-STATUS-BIT DEFINITIONS

The alarm-status bits indicate the FPU-16 alarm conditions.

ALARM-STATUS BITS	
BIT NUMBER	ALARM FUNCTION
0 (LSB)	1 = I ² t Alarm
1	1 = Short-Time Alarm
2	1 = Instantaneous Alarm
3	1 = Unbalance Alarm
4	1 = Earth-fault Alarm
5	Not Used
6	Not Used
7	1 = Memory-Fault Alarm

TABLE 5

5.1.6 FPU-16 STATUS DEFINITIONS

These bits define the FPU status.

MOTOR-STATUS BITS	
BIT NUMBER	FUNCTION
0 (LSB)	1 = Load Current > 10%
1	1 = Contact Closed, 0 = Contact Open

TABLE 6

6. FPU-16 DATA LOGGING OPTION

The FPU-16 data logger captures time-stamped meter data using either a time or event trigger mechanism. Captured records are stored in non-volatile memory, which has a data retention of at least 10 years. The real-time clock (RTC) continues to operate even without control voltage.

Configuration registers are used to configure the data logger. The same command format as described in section 4 is used for data logger communication. Unlike the set point and reset memory however, the data logger allows for multiple writes to the configuration registers.

6.1 CONFIGURATION REGISTERS

Table 7 shows the Modbus and register address location of each configuration register.

CONFIGURATION REGISTERS			
MODBUS ADDRESS	REGISTER ADDRESS	DESCRIPTION	
40129	0x80	MSB: N/A	LSB: Year
40130	0x81	MSB: Month	LSB: Date
40131	0x82	MSB: Day	LSB: Hour
40132	0x83	MSB: Minute	LSB: Second
40133	0x84	Sample Interval in Seconds	
40134	0x85	Trigger Duration Count	
40135	0x86	Control	
40136	0x87	Trip Status Trigger Mask	
40137	0x88	Alarm Status Trigger Mask	
40138	0x89	FPU-16 Status Trigger Mask	
40139	0x8A	Record Counter (Read Only)	

TABLE 7

6.2 REGISTER DEFINITIONS

16-bit registers are used to configure the data logger.

40129: (read/write)

NOT USED (Bits 8:15)	YEAR (Bits 0:7)
----------------------	-----------------

YEAR: 00 to 99 BCD

40130: (read/write)

MONTH (Bits 8:15)	DATE (Bits 0:7)
-------------------	-----------------

MONTH: 01 to 12 BCD

DATE: 01 to 31 BCD

40131: (read/write)

DAY (Bits 8:15)	HOUR (Bits 0:7)
-----------------	-----------------

DAY: 01 to 07 BCD

HOUR: 00 to 23 BCD

40132: (read/write)

MINUTE (Bits 8:15)	SECOND (Bits 0:7)
--------------------	-------------------

MINUTES: 00 to 59 BCD

SECONDS: 00 to 59 BCD

40133: (read/write)

SAMPLE INTERVAL IN SECONDS (Bits 0:15)
--

SAMPLE INTERVAL: 1 to 65536 Seconds

A sample interval of 0 is not valid.

40134: (read/write)

POST-TRIGGER DURATION (Bits 0:7)

POST-TRIGGER DURATION: 0 to 249 (Valid in Event Mask trigger mode only.).

The duration count specifies the number of additional records captured after an event-trigger occurs. The time between records is defined by the sample interval.

If a trigger occurs while the duration counter is active, this record will be captured but the duration count will not be initialized. The duration count is initialized only at the occurrence of the first event.

40135: (read/write)

	CLOCK ENABLE (Bit 4)	CLEAR COUNTER (Bit 3)	MODE (Bits 0:2)
--	----------------------	-----------------------	-----------------

CONTROL REGISTER:

MODE:

- 0: Disable data logging.
- 1: Set trigger to TIME and start recording.
- 2: Set trigger to EVENT MASK mode and enable trigger.
- 3 to 7: Not Used.

CLEAR COUNTER:

- 0: The record counter is not cleared.
- 1: The record counter is cleared.

This bit is cleared by the data logger when the counter has been cleared.

CLOCK ENABLE:

- 0: Clock OSC is turned off. (RTC not running)
- 1: Clock OSC is on.

40136: (read/write)

16-Bit Trip Status Trigger Mask (Bits 0:15)

TRIP STATUS TRIGGER MASK: Bits that are set in the mask register enables triggering for the corresponding trip-status bit. For triggering to occur, the selected trip-status bits must be all zero prior to one of the bits going high.

40137: (read/write)

16-Bit Alarm Status Trigger Mask (Bits 0:15)

ALARM STATUS TRIGGER MASK: Bits that are set in the mask register enables triggering for the corresponding alarm-status bit. For triggering to occur, the selected alarm-status bits must be all zero prior to one of the bits going high.

40138: (read/write)

16-Bit FPU-16 Status Trigger Mask (Bits 0:15)

FPU-16 STATUS TRIGGER MASK: Bits that are set in the mask register enables triggering for the corresponding FPU-16 status bit. If any of the enabled bits changes state, triggering occurs.

40139: (read only)

Record Counter

RECORD COUNTER: Counts the number of records captured. This is a read-only location and is cleared by using the control register.

6.3 TRIGGER DESCRIPTION

With the trigger mode set to TIME, the data logger stores records at fixed time intervals. The time is defined by SAMPLE INTERVAL. In the TIME mode, any trip, alarm or FPU-16 status that matches the mask bits will also be recorded. TRIGGER DURATION does not apply in TIME mode. When the number of records exceeds 250, new records overwrite old records.

With the trigger mode set to EVENT MASK, the data logger will trigger on a specific trip, alarm or FPU-16 status condition. The trigger-mask bits define which trip, alarm or FPU-16 status bits will initiate the trigger. Event mask bit locations correspond to the trip-status, alarm-status, and FPU-16 status bits defined in the communications protocol. To enable triggering on a status bit, the corresponding mask bit is set. All selected bits in the trip or alarm status must be zero to arm the trigger. When any or all of the bits in the trip or alarm status transition from zero to one, the data-logger will be triggered. When triggered, the data logger will store the number of records defined by TRIGGER DURATION with a time interval defined by the sample unit/interval settings. In the case of the FPU-16 status, not all bits have to be zero to arm the trigger. Any bit that changes status will cause a trigger. While in "trigger-duration" mode, event triggering is active, however the duration counter is initialized on the first trigger condition.

6.4 DATA-LOGGING RECORD FORMAT

Up to 250 records are stored in non-volatile memory. These records are read-only and are retrieved by specifying the starting address and length for the record. Each record requires a separate read request. The first record (record 0) is always the latest record, and record 249 is always the last record. Each record consists of the following data (Record 0 addresses shown):

DATA LOGGER RECORD FORMAT

MODBUS ADDRESS	REGISTER ADDRESS	DESCRIPTION
40193	0xC0	MSB: N/A LSB: Year MSB: Month LSB: Date MSB: Day LSB: Hour MSB: Minute LSB: Second Trip Status Alarm Status FPU-16 Status Phase A (A) Phase B (A) Phase C (A) Earth Leakage (x10 A) I ² t (%) Operations Count Pre-Trip Phase A (A) Pre-Trip Phase B (A) Pre-Trip Phase C (A) Pre-Trip Unbalance (%) Pre-Trip Earth Leakage (x10 A) Pre-trip I ² t (%)

TABLE 8

The starting address for a record is defined by:

$$\text{Modbus Address} = 40193 + (\text{Record_Number} * 24) \text{ or}$$

$$\text{Register Address} = 0xC0 + (\text{Record_Number} * 24)$$

Where Record_Number=0 is the latest record.

NOTE: The record length is a maximum of 24 words or 48 bytes.

7. FPU-16 STATION-ADDRESS SELECTION

The second level of the Mode-5 program option is used to specify the FPU-16 station address.

Value digits 2 and 3 indicates a decimal address from 0 to 63. Address 0 is the default value and inhibits serial communication.

Value digit 1 indicates the relay-operating mode.

MODE-5 PROGRAM OPTIONS (2nd Level)

DEFAULT VALUE 5000

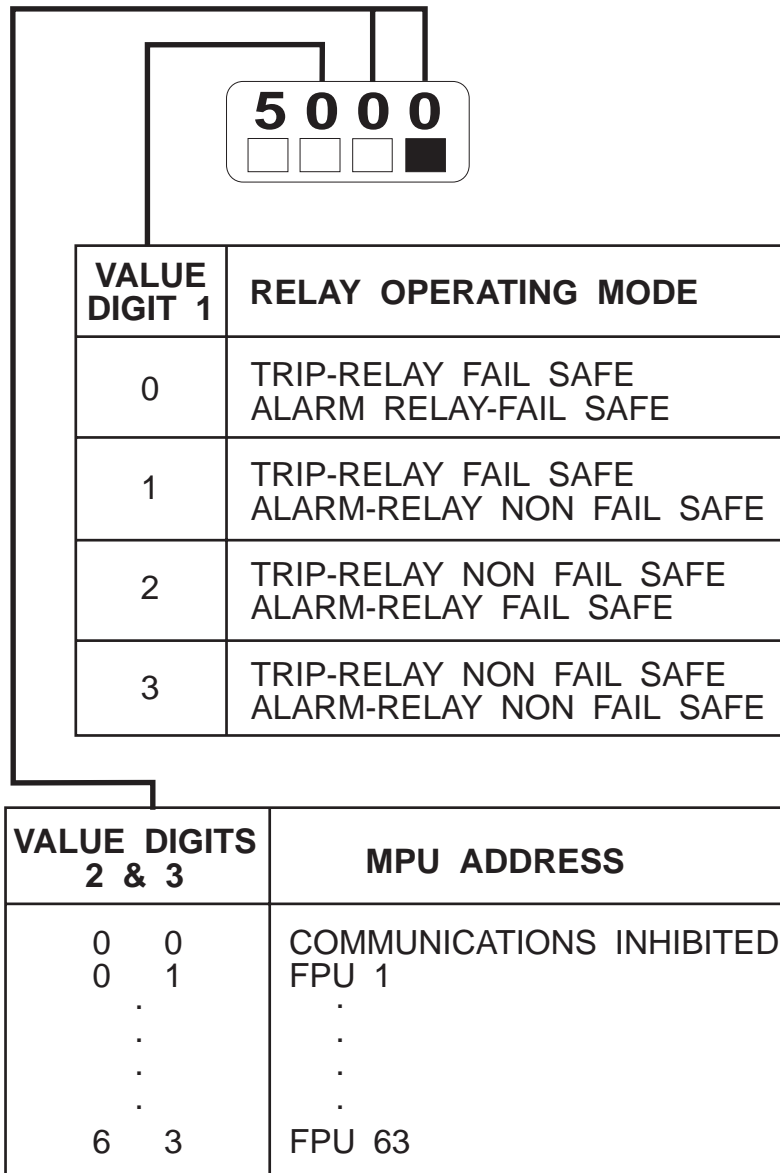


TABLE 9

The FPU-16 supports the Modbus Broadcast Address for write commands only. Any FPU-16 that is not inhibited (address not zero) will execute broadcast commands.

8. CONFIGURATION SWITCHES

Eight DIP switches are located on the back of the communications card. The DIP switches are accessible through the slot on the back of the FPU-16. When viewed from the rear, SW1 is the right-most switch. A switch is CLOSED when the actuator is up (toward the PCB) and OPEN when the actuator is down (away from the PCB).

Switches 1 to 3 are used to select the communication baud rate.

BAUD RATE

BAUD	SW1	SW2	SW3	SW4 - SW8
9600	OPEN	CLOSED	OPEN (DEFAULT)	NOT USED
4800	CLOSED	CLOSED	OPEN	
2400	OPEN	OPEN	CLOSED	
1200	CLOSED	OPEN	CLOSED	
600	OPEN	CLOSED	CLOSED	
300	CLOSED	CLOSED	CLOSED	

NOTE: SW6 is used for software-update programming and MUST be in the OPEN position for normal communications. SW4, SW5, SW7, and SW8 are not used.

TABLE 10

The FPU-16 RS-485 port is fixed at 8 data bits, 1 stop bit, and no parity.

9. SPECIFICATIONS

Interface	Isolated RS-485, 2 wire multi-drop, half duplex.
Protocol	Modbus RTU
Baud Rate	300 to 9600 Baud.
Bit Format.....	8 bits, no parity, one stop bit.*
Number of FPU's Connected.....	Maximum of 31 units.◆
Line length.....	1200 meters total.
Isolation Voltage.....	300 Vac continuous
Dielectric.....	1500 Vac

* Terminal 23 (-) is negative with respect to terminal 24 (+) for a binary 1 (MARK or OFF) state.

Terminal 23 (-) is positive with respect to terminal 24 (+) for a binary 0 (SPACE or ON) state.

◆ Can be expanded to 62 units with repeater connection.

10. INTERFACE CONVERTER

A communication master with a RS-232 port requires an RS-232 to RS-485 converter. Two types of converters are available and converter selection depends upon the hardware/software configuration of the master.

The first type uses hardware control where the RTS line of the RS-232 is used to control the transmit and receive mode of the RS-485 transceiver. When the RTS line is high, the transmitter is enabled and when it is low, the transmitter is disabled and the receiver is enabled. Usually the master software must be specifically designed for use with this type of control. This type of converter is the most common type; however, most software packages do not support the hardware handshaking control.

The second type is the "data only" converter. This converter monitors the data from the master and sets the transmitter ON or OFF based on activity on the line. This type of converter requires time to switch from transmit to receive mode. To avoid RS-485 data collision, a reply or turn-around delay is required at the slave. This type of converter will work with all software packages that support a master/slave, half-duplex protocol.

The recommended converter is the Model 485COSR or 485CSP manufactured by B&B Electronics, and are available from Startco Engineering Ltd. These converters are "data-only" converters and are configured for operation at 9600 baud. Slower rates require modification to the converter. Consult the factory for operation below 9600 baud.

10.1 NETWORK INTERCONNECTION

A general diagram is shown in Figure 6 with more detailed wiring diagrams shown in Figures 4 and 5.

FPU-16 communication ports are interconnected using a two-wire twisted pair cable. Communication ports are connected in a daisy-chain method. All FPU-16 + terminals are connected to the white wire, and all FPU-16 - terminals to the black wire. In the case of the 485CSP, the + terminal is connected too the (B) terminal and the - terminal to the (A) terminal.

The Model 485COSR and 485CSP are provided with a DB25 connector on the RS-232 side and a terminal block for the RS-485 side. The RS-232 connector is the same for both the 485CSP and 485COSR and is a female connector with the following pins supported.

<u>Pin #</u>	<u>Description</u>
1	Shield ground
2	Data to converter from computer
3	Data from converter to computer
7	Signal ground

The RS-485 connector is a terminal block with the following designations:

485CSP ADAPTER DESCRIPTION	485COSR ADAPTER DESCRIPTION
FR Shield Ground	+ (RS485 Positive)
TDA RS485 (-)	- (RS485 Negative)
TDB RS485 (+)	
RDA RS485 (-)	
RDB RS485 (+)	
Signal Ground	
Remote Power (+) 12 V	
Remote Power (-) GND	

If the converter is at one end of the network, a 150 ohm termination is connected between (-) and (+) on this connector.

Power for the converter is supplied by an "adapter-type" power supply (Model 485PS) which connects to the + and - terminals of the terminal block.

10.2 RS-485 TERMINATION

Termination resistors are required for line lengths greater than 25 meters. Termination resistors are normally selected to match the characteristic impedance of the communication line, and are installed at each end of the network.

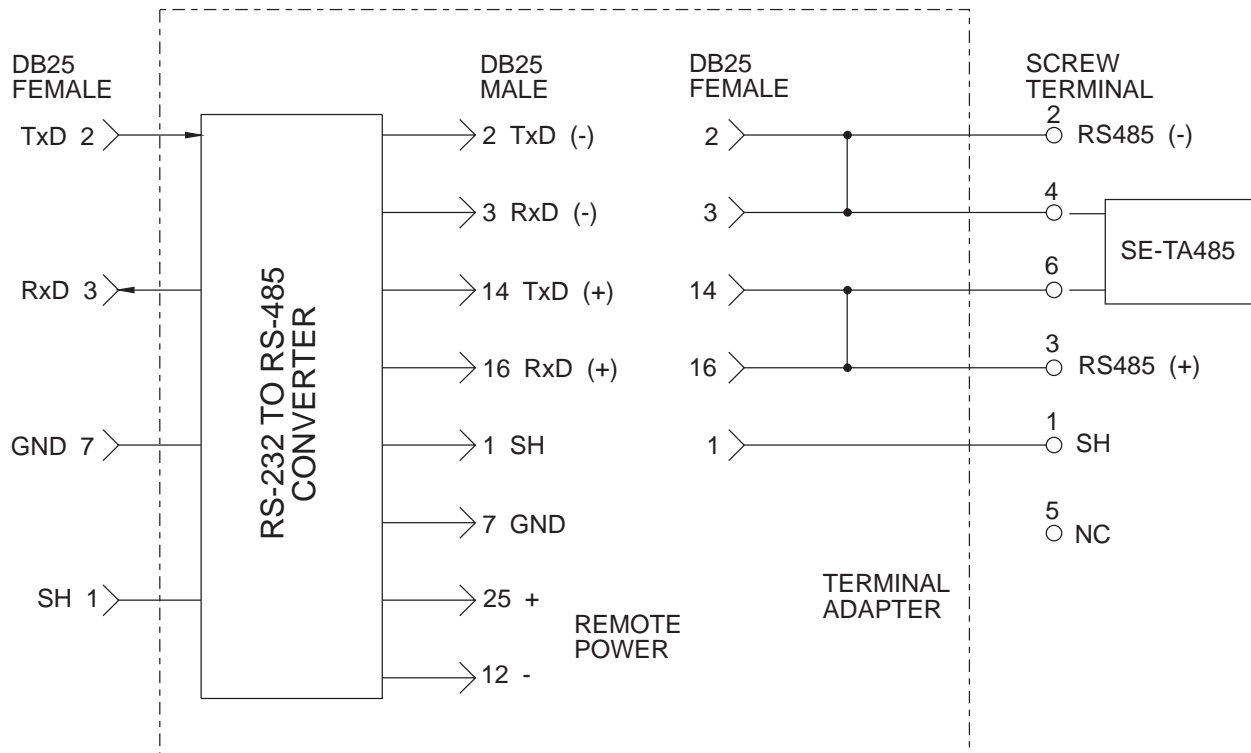
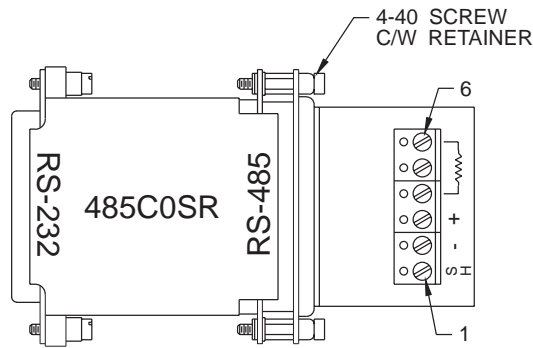
When the RS-485 line is idle, all of the RS-485 devices are in a receive state. Since the line is not driven, the voltage across the twisted-pair cable is zero. This results in an unknown output state on the master's RS-485 converter which can cause communication problems with the master software.

To force the RS-485 line to a known state, each FPU-16 has a 100K pull-up resistor connected from the internal 5-volt supply to the (+) line and a 100K pull-down resistor connected from the (-) terminal to internal circuit ground.

The combination of the pull-up, pull-down, and termination resistances results in a voltage on the RS-485 line that must be greater than the 200 mV threshold of the RS-485 receiver to guarantee a valid idle state.

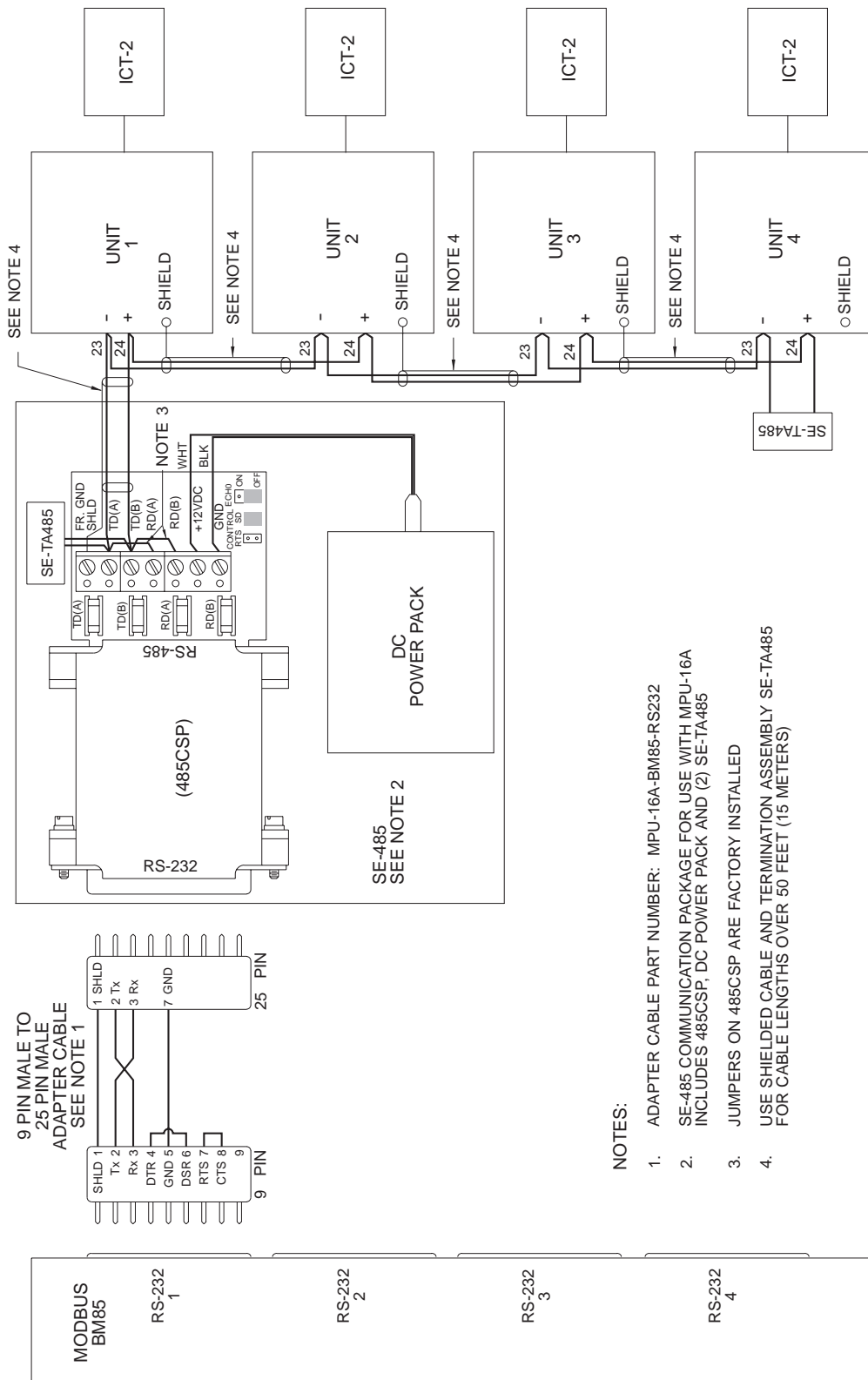
For the RS-485 network used with the FPU-16, the termination consists of a 150 ohm resistor in series with a 0.1 mf capacitor.

This combination satisfies the valid idle-state requirements and provides the 150 ohm termination for the cable.



RS-232 TO RS-485 CONVERTER

FIGURE 5



NOTES:

1. ADAPTER CABLE PART NUMBER: MPU-16A-BM85-RS232
2. SE-485 COMMUNICATION PACKAGE FOR USE WITH MPU-16A INCLUDES 485CSP, DC POWER PACK AND (2) SE-TA485
3. JUMPERS ON 485CSP ARE FACTORY INSTALLED
4. USE SHIELDED CABLE AND TERMINATION ASSEMBLY SE-TA485 FOR CABLE LENGTHS OVER 50 FEET (15 METERS)

DETAILED APPLICATION USING MODBUS PLC

FIGURE 6