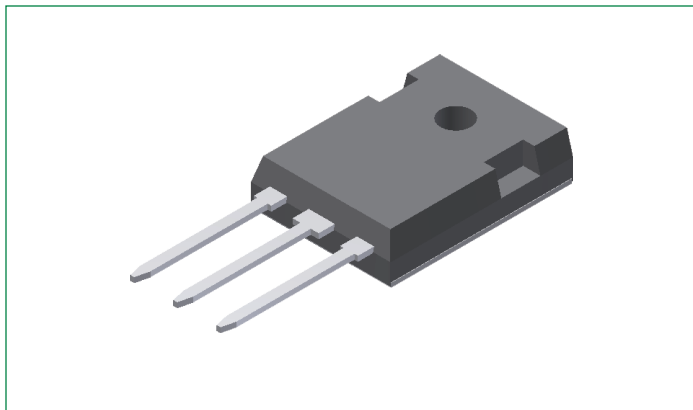


CLA50E1200HB

1200 V, 50 A High Efficiency Thyristor

RoHS



Features:

- Thyristor for line frequency
- Long-term stability
- Planar passivated chip

Applications:

- Line rectifying 50/60 Hz
- DC motor control
- Soft start AC motor control
- Power converter
- Lighting and temperature control
- AC power control

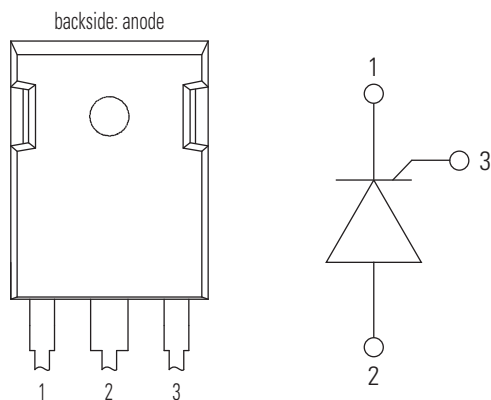
Package:

- RoHS compliant
- Industry standard TO-247 package
- Epoxy meets UL 94V-0

Product Summary

Characteristic	Value	Unit
V_{RRM}	1200	V
I_{TAV}	50	A
V_T	1.27	V

Pinout Diagram (TO-247-3L)



1: Cathode; 2: Anode; 3: Gate

Maximum Ratings

Symbol	Characteristics	Conditions		Value	Units
$I_{T(RMS)}$	RMS On-state Current (Half Sine Wave)	180° Sine; $T_C = 125^{\circ}C$; $T_{VJ} = 150^{\circ}C$		79	A
I_{TAV}	Average Forward Current			50	
$I_{R/D}$	Reverse Current, Drain Current	$T_{VJ} = 25^{\circ}C$; $V_{R/D} = 1200\text{ V}$		50	μA
		$T_{VJ} = 125^{\circ}C$; $V_{R/D} = 1200\text{ V}$		4	mA
I_{TSM}	Maximum Forward Surge Current	$T_{VJ} = 45^{\circ}C$	t = 10 ms, 50 Hz sine, $V_R = 0\text{ V}$	650	A
			t = 8.3 ms, 60 Hz sine, $V_R = 0\text{ V}$	700	
		$T_{VJ} = 150^{\circ}C$	t = 10 ms, 50 Hz sine, $V_R = 0\text{ V}$	555	
			t = 8.3 ms, 60 Hz sine, $V_R = 0\text{ V}$	595	
I^2t	I^2t Value for Fusing	$T_{VJ} = 45^{\circ}C$	t = 10 ms, 50 Hz sine, $V_R = 0\text{ V}$	2.12	kA ² s
			t = 8.3 ms, 60 Hz sine, $V_R = 0\text{ V}$	2.04	
		$T_{VJ} = 150^{\circ}C$	t = 10 ms, 50 Hz sine, $V_R = 0\text{ V}$	1.54	
			t = 8.3 ms, 60 Hz sine, $V_R = 0\text{ V}$	1.48	
V_{RSM}/V_{DSM}	Maximum Non-repetitive Reverse/Forward Blocking Voltage	$T_{VJ} = 25^{\circ}C$		1300	V
V_{RRM}/V_{DRM}	Maximum Repetitive Reverse/Forward Blocking Voltage	$T_{VJ} = 25^{\circ}C$		1200	V
di/dt_{cr}	Critical Rate of Rise of On-state Current	$t_p = 200\text{ }\mu s$; f = 50 Hz; $di_G/dt = 0.3\text{ A}/\mu s$; $I_G = 0.3\text{ A}$; $T_{VJ} = 150^{\circ}C$; $V = 2/3 V_{DRM}$	Repetitive, $I_T = 150\text{ A}$	150	A/ μs
			Non-repetitive, $I_T = 50\text{ A}$	500	
dv/dt_{cr}	Critical Rate of Rise of Voltage	$V = 2/3 V_{DRM}$, $R_{GK} = \infty$, method 1 (linear voltage rise), $T_{VJ} = 150^{\circ}C$		1000	V/ μs
P_{GM}	Maximum Gate Power Dissipation	$T_C = 150^{\circ}C$	$t_p = 30\text{ }\mu s$	10	W
			$t_p = 300\text{ }\mu s$	5	
P_{GAV}	Average Gate Power Dissipation	$T_C = 150^{\circ}C$		0.5	W
P_{tot}	Total Power Dissipation	$T_C = 25^{\circ}C$		500	W
T_{STG}	Storage Temperature Range	–		–40 to 150	$^{\circ}C$
T_{OP}	Operating Temperature Range	–		–40 to 125	$^{\circ}C$
T_{VJ}	Virtual Junction Temperature Range	–		–40 to 150	$^{\circ}C$

Thermal Characteristics

Symbol	Characteristics	Value			Units
		Min.	Typ.	Max.	
R_{thJC}	Thermal Resistance, Junction to Case	–	–	0.25	K/W
R_{thCH}	Thermal Resistance, Case to Heatsink	–	0.3	–	K/W

Electrical Characteristics

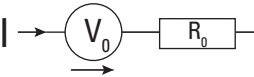
Symbol	Characteristics	Conditions		Value			Units
				Min.	Typ.	Max.	
I _{GT}	Gate Trigger Current	T _{VJ} = 25°C	V _D = 6 V	–	–	50	mA
		T _{VJ} = –40°C		–	–	80	
V _{GT}	Gate Trigger Voltage	T _{VJ} = 25°C	V _D = 6 V	–	–	1.5	V
		T _{VJ} = –40°C		–	–	1.6	
I _{GD}	Gate Non-trigger Current	V _D = 2/3 V _{DRM} , T _{VJ} = 150°C		–	–	3	mA
V _{GD}	Gate Non-trigger Voltage	V _D = 2/3 V _{DRM} , T _{VJ} = 150°C		–	–	0.2	V
V _T	Forward Voltage Drop	T _{VJ} = 25°C	I _T = 50 A	–	–	1.32	V
			I _T = 100 A	–	–	1.60	
		T _{VJ} = 125°C	I _T = 50 A	–	–	1.27	
			I _T = 100 A	–	–	1.65	
I _L	Latching Current	t _p = 10 μs; I _G = 0.3 A; di _G /dt = 0.3 A/μs; T _{VJ} = 25°C		–	–	125	mA
I _H	Holding Current	V _D = 6 V; R _{GK} = ∞; T _{VJ} = 25°C		–	–	115	mA
V _{T0}	Threshold Voltage ¹	T _{VJ} = 150°C		–	–	0.88	V
r _T	Slope Resistance ¹	T _{VJ} = 150°C		–	–	7.7	mΩ
C _J	Junction Capacitance	V _R = 400 V, f = 1 MHz		–	25	–	pF
t _{gd}	Gate Controlled Delay Time	V _D = 1/2 V _{DRM} ; I _G = 0.3 A ; di _G /dt = 0.3 A/μs; T _{VJ} = 25°C		–	–	2	μs
t _q	Turn-off Time	V _R = 100 V; I _T = 50 A; V = 2/3 V _{DRM} ; di/dt = 10 A/μs; dv/dt = 20 V/μs; t _p = 200 μs; T _{VJ} = 125°C		–	200	–	μs

Note 1: For power loss calculation only

Package

Symbol	Characteristics	Conditions	Value			Units
			Min.	Typ.	Max.	
I _{RMS}	RMS Current	per terminal	–	–	70	A
M _D	Mounting Torque	–	0.8	–	1.2	Nm
F _C	Mounting force with clip	–	20	–	120	N
G	Weight	–	–	6	–	g

Equivalent Circuits for Simulation (T_{VJ} = 150°C)



Symbol	Characteristics	Value	Units
V _{0 max}	Threshold Voltage	0.88	V
R _{0 max}	Slope Resistance ¹	5.2	mΩ

Note 1: On die level

Characteristic Curves

Figure 1. Forward Characteristics

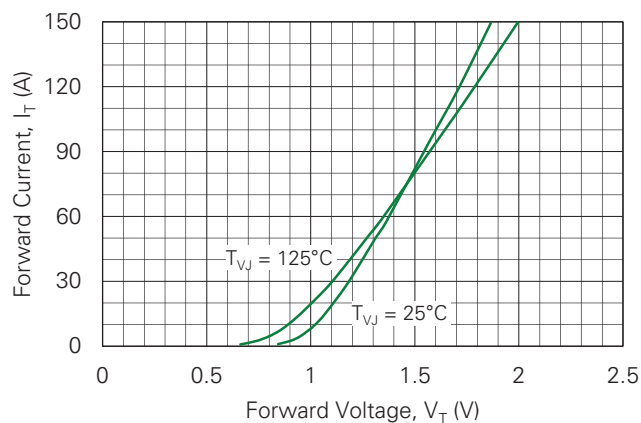


Figure 2. Surge Overload Current

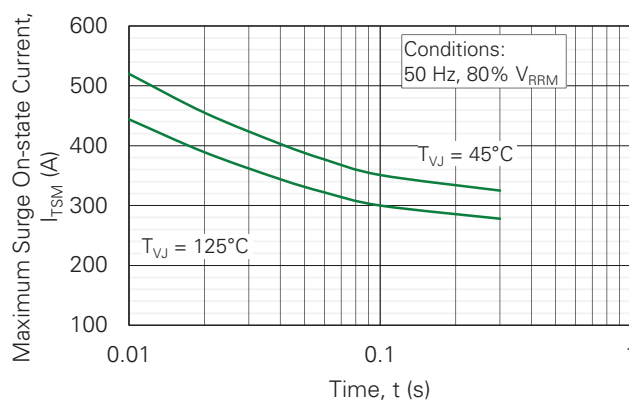
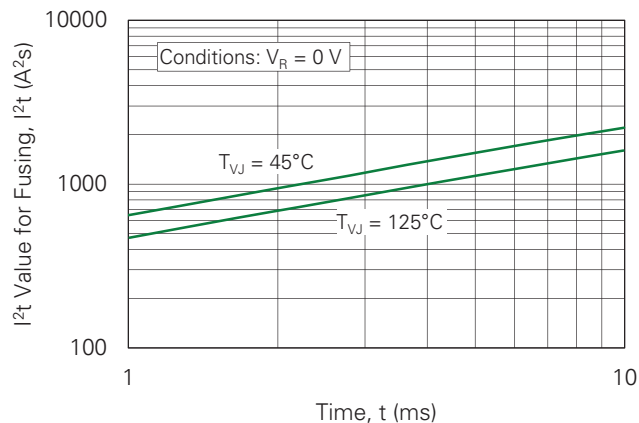
 I_{TSM} : Crest Value, t : durationFigure 3. I^2t vs. Time (1-10 s)

Figure 4. Gate Trigger Voltage vs. Gate Trigger Current

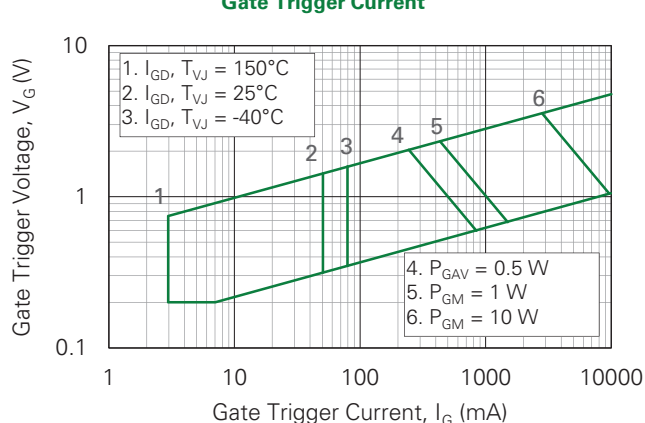


Figure 5. Gate Controlled Delay Time vs. Gate Trigger Current

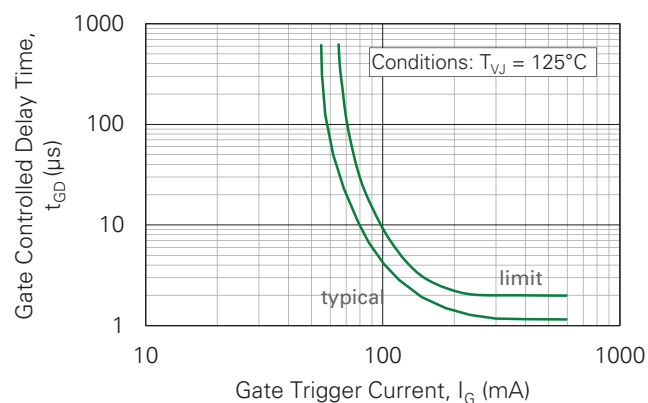


Figure 6. Max. Forward Current vs. Case Temperature

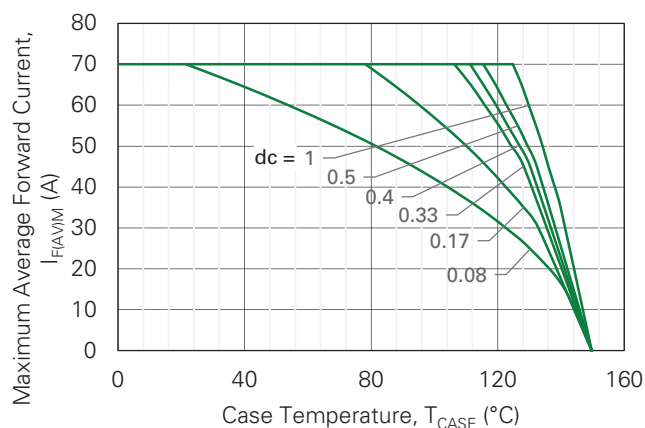


Figure 7a. Power Dissipation vs. Direct Output Current

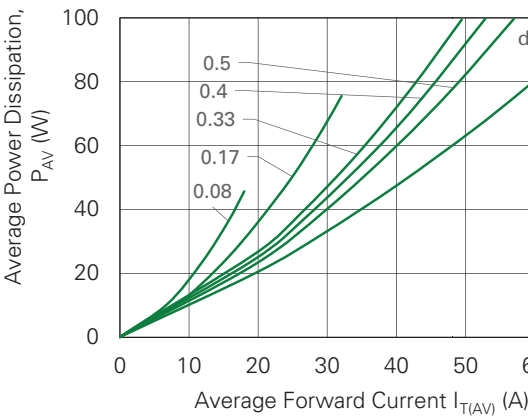


Figure 7b. Power Dissipation vs. Ambient Temperature

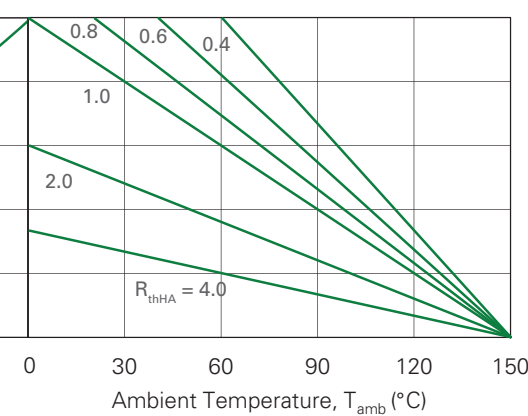
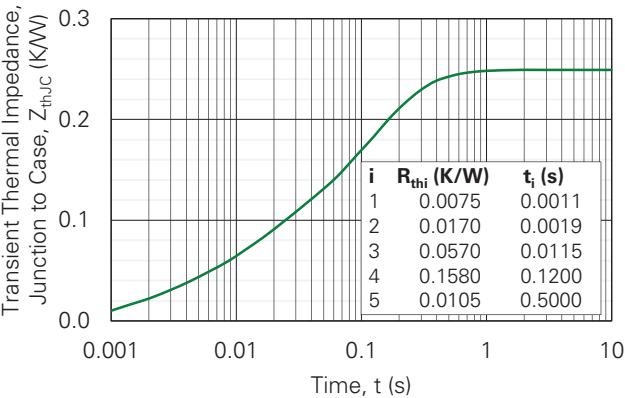
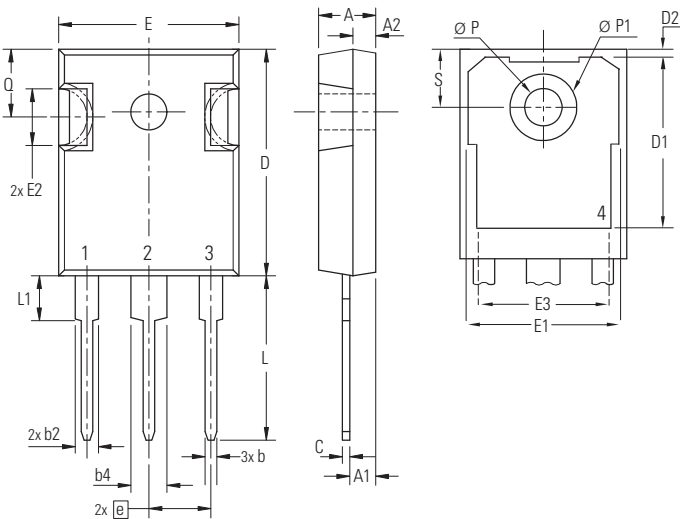


Figure 8. Transient Thermal Impedance, Junction to Case



Part Outline Drawing (TO-247-3L)



Symbol	Millimeters		Inches	
	Min.	Max.	Min.	Max
A	4.70	5.30	0.185	0.209
A1	2.21	2.59	0.087	0.102
A2	1.50	2.49	0.059	0.098
b	0.99	1.40	0.039	0.055
b2	1.65	2.39	0.065	0.094
b4	2.59	3.43	0.102	0.135
C	0.38	0.89	0.015	0.035
D	20.79	21.45	0.819	0.845
D1	13.07	—	0.515	—
D2	0.51	1.35	0.020	0.053
e	5.45 BSC		0.215 BSC	
E	15.48	16.24	0.610	0.640
E1	13.45	—	0.530	—
E2	4.31	5.48	0.170	0.216
E3	—	13.43	—	0.529
L	19.80	20.30	0.780	0.800
L1	—	4.49	—	0.177
Q	5.38	6.19	0.212	0.244
S	6.14 BSC		0.242 BSC	
ØP	3.55	3.65	0.140	0.144
ØP1	—	7.39	—	0.29

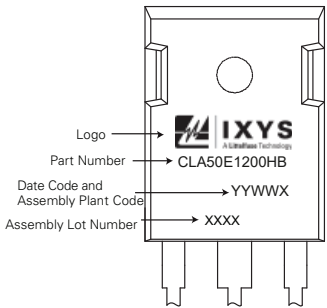
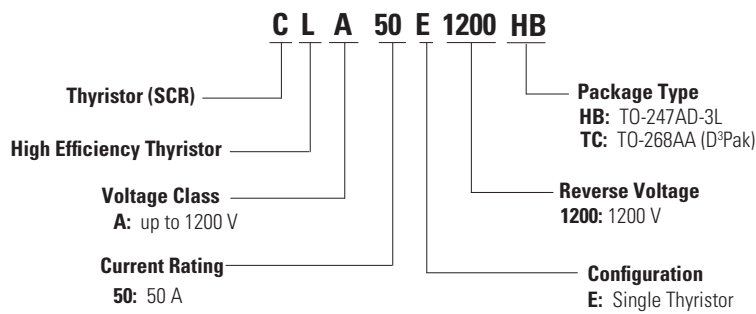
Product Selector

Part Number	Voltage Class	Package
CLA50E1200HB	1200 V	TO-247AD-3L
CLA50E1200TC	1200 V	TO-268AA (D ³ PAK)

Packing Options

Part Number	Marking	Packing Mode	Quantity
CLA50E1200HB	CLA50E1200HB	Tube	30

Part Numbering and Marking



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