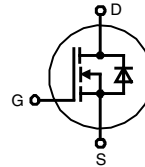


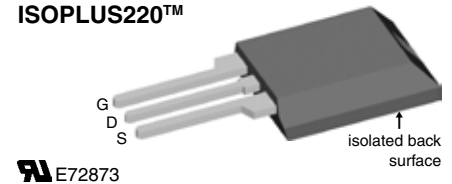
CoolMOS™ 1) Power MOSFET

Electrically isolated back surface
2500 V electrical isolation
N-Channel Enhancement Mode
Low $R_{DS(on)}$, high V_{DSS} MOSFET
Ultra low gate charge

$$\begin{aligned} I_{D25} &= 23 \text{ A} \\ V_{DSS} &= 600 \text{ V} \\ R_{DS(on) \text{ max}} &= 0.1 \Omega \end{aligned}$$



ISOPLUS220™



Preliminary data

MOSFET				
Symbol	Conditions	Maximum Ratings		
V_{DSS}	$T_{VJ} = 25^\circ\text{C}$	600		V
V_{GS}		± 20		V
I_{D25}	$T_C = 25^\circ\text{C}$	23		A
I_{D90}	$T_C = 90^\circ\text{C}$	16		A
E_{AS}	single pulse } $I_D = 11 \text{ A}; T_C = 25^\circ\text{C}$	800		mJ
E_{AR}		1.2		mJ
dV/dt	MOSFET dV/dt ruggedness $V_{DS} = 0 \dots 480 \text{ V}$	50		V/ns

Symbol	Conditions	Characteristic Values			
		$(T_{VJ} = 25^\circ\text{C}, \text{ unless otherwise specified})$			
		min.	typ.	max.	
$R_{DS(on)}$	$V_{GS} = 10 \text{ V}; I_D = 18 \text{ A}$		90	100	m Ω
$V_{GS(th)}$	$V_{DS} = V_{GS}; I_D = 1.2 \text{ mA}$	2.5	3	3.5	V
I_{DSS}	$V_{DS} = 600 \text{ V}; V_{GS} = 0 \text{ V}$			5	μA
	$T_{VJ} = 125^\circ\text{C}$		50		μA
I_{GSS}	$V_{GS} = \pm 20 \text{ V}; V_{DS} = 0 \text{ V}$			100	nA
C_{iss}	$V_{GS} = 0 \text{ V}; V_{DS} = 100 \text{ V}$		2800		pF
C_{oss}			130		pF
Q_g	$V_{GS} = 0 \text{ to } 10 \text{ V}; V_{DS} = 400 \text{ V}; I_D = 18 \text{ A}$		60	80	nC
Q_{gs}			14		nC
Q_{gd}			20		nC
$t_{d(on)}$	$V_{GS} = 10 \text{ V}; V_{DS} = 400 \text{ V}$		10		ns
t_r			5		ns
$t_{d(off)}$			60		ns
t_f			5		ns
R_{thJC}				0.85	K/W

Features

- Silicon chip on Direct-Copper-Bond substrate
 - high power dissipation
 - isolated mounting surface
 - 2500 V electrical isolation
 - low drain to tab capacitance ($< 30 \text{ pF}$)
- Fast CoolMOS™ 1) power MOSFET 4th generation
 - high blocking capability
 - lowest resistance
 - avalanche rated for unclamped inductive switching (UIS)
 - low thermal resistance due to reduced chip thickness
- Enhanced total power density

Applications

- Switched mode power supplies (SMPS)
- Uninterruptible power supplies (UPS)
- Power factor correction (PFC)
- Welding
- Inductive heating
- PDP and LCD adapter

Advantages

- Easy assembly: no screws or isolation foils required
- Space savings
- High power density
- High reliability

1) CoolMOS™ is a trademark of Infineon Technologies AG.

Source-Drain Diode

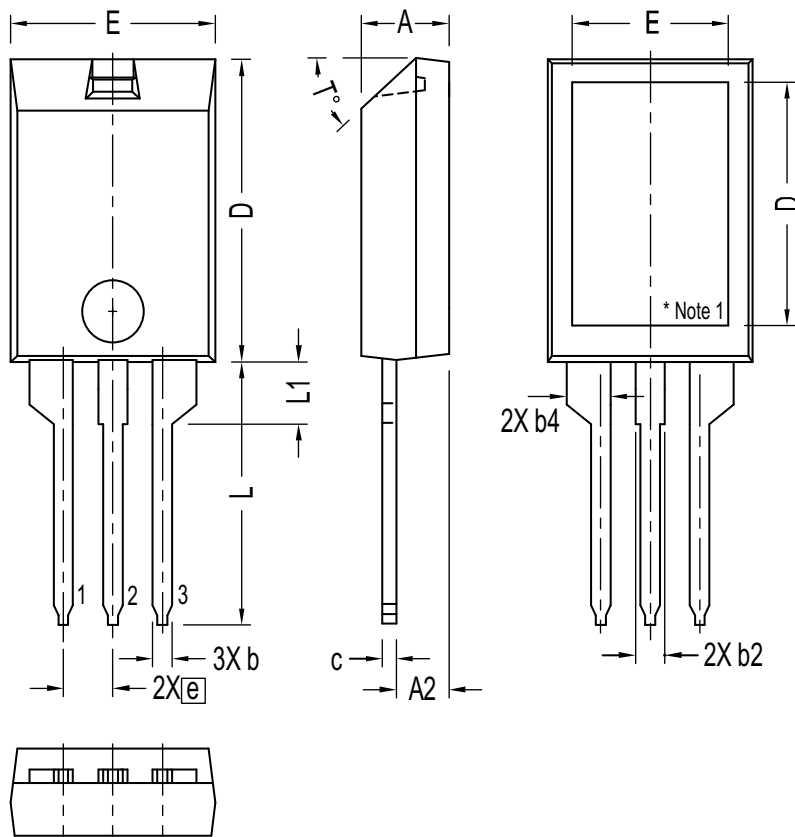
Symbol	Conditions	Characteristic Values			
		min.	typ.	max.	
I_S	$V_{GS} = 0\text{ V}$			16	A
V_{SD}	$I_F = 16\text{ A}; V_{GS} = 0\text{ V}$		0.9	1.2	V
t_{rr}	$I_F = 16\text{ A}; -di_F/dt = 100\text{ A}/\mu\text{s}; V_R = 400\text{ V}$		450		ns
Q_{RM}			12		μC
I_{RM}			70		A

Component

Symbol	Conditions	Maximum Ratings	
T_{VJ}	operating	-55...+150	°C
T_{stg}	storage	-55...+150	°C
V_{ISOL}	RMS leads-to-tab, 50/60 Hz, $f = 1\text{ minute}$	2500	V~
F_C	mounting force	11-65 / 2.4-11	N/lb

Symbol	Conditions	Characteristic Values		
		min.	typ.	max.
R_{thCH}	with heatsink compound		0.28	K/W
Weight			3.1	g

ISOPLUS220™ Outline



SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.157	.197	4.00	5.00
A2	.098	.118	2.50	3.00
b	.035	.051	0.90	1.30
b2	.049	.065	1.25	1.65
b4	.093	.100	2.35	2.55
c	.028	.039	0.70	1.00
D	.591	.630	15.00	16.00
D1	.472	.512	12.00	13.00
E	.394	.433	10.00	11.00
E1	.295	.335	7.50	8.50
e	.100 BASIC		2.55 BASIC	
L	.512	.571	13.00	14.50
L1	.118	.138	3.00	3.50
T°			42.5°	47.5°

NOTE:

1. Bottom heatsink is electrically isolated from Pin 1, 2, or 3.
2. This drawing will meet dimensional requirement of JEDEC SS Product Outline TO-273 except D and D1 dimension.

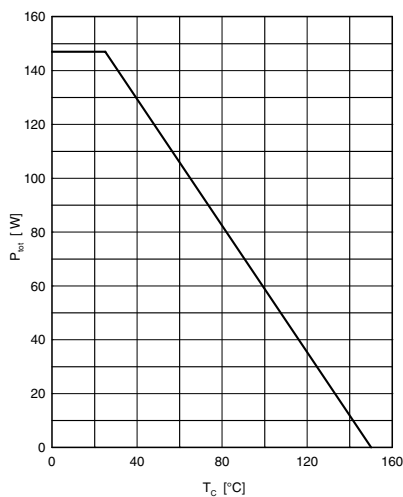


Fig. 1 Power dissipation

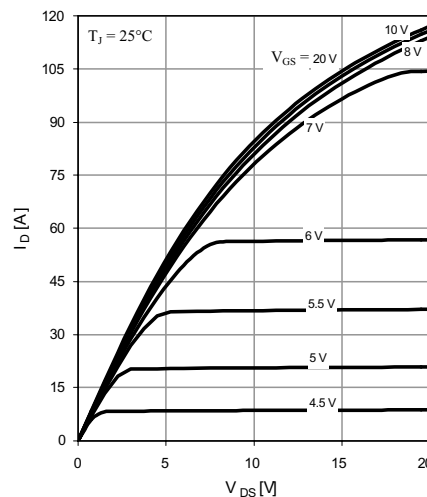


Fig. 2 Typ. output characteristics

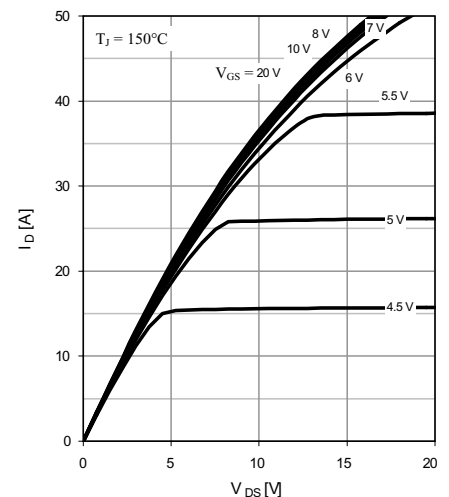


Fig. 3 Typ. output characteristics

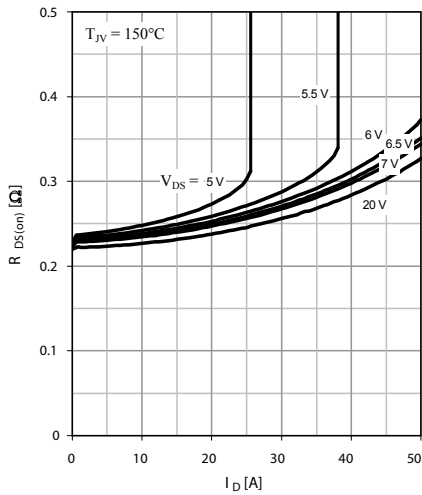


Fig. 4 Typ. drain-source on-state resistance characteristics

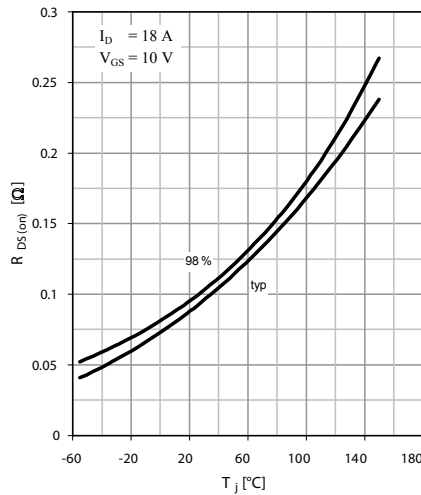


Fig. 5 Drain-source on-state resistance

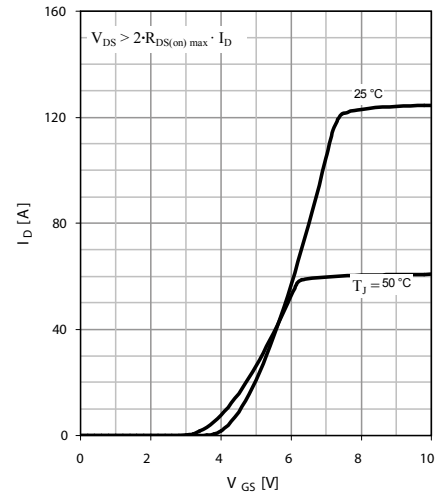


Fig. 6 Typ. transfer characteristics

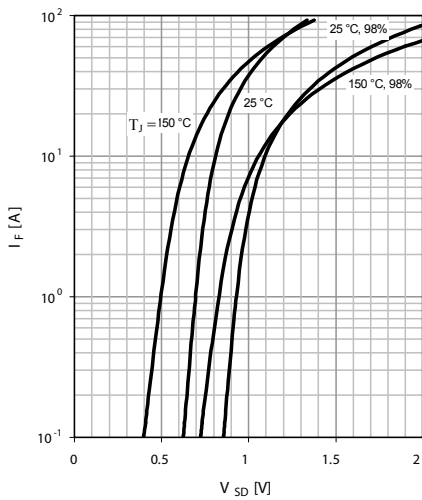


Fig. 7 Forward characteristic of reverse diode

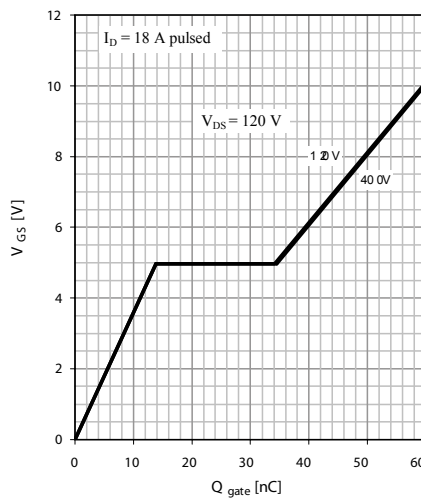


Fig. 8 Typ. gate charge

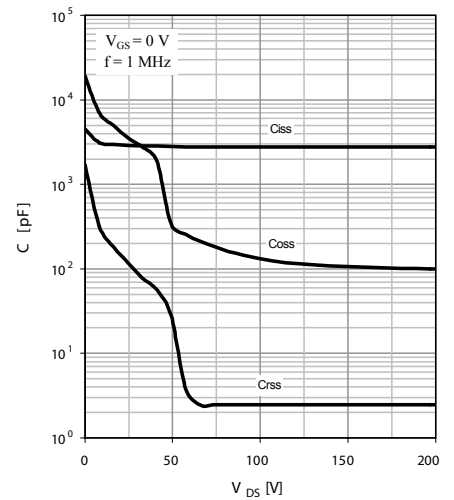


Fig. 9 Typ. capacitances

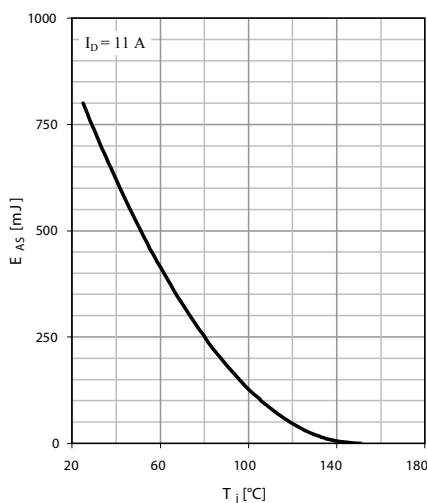


Fig. 10 Avalanche energy

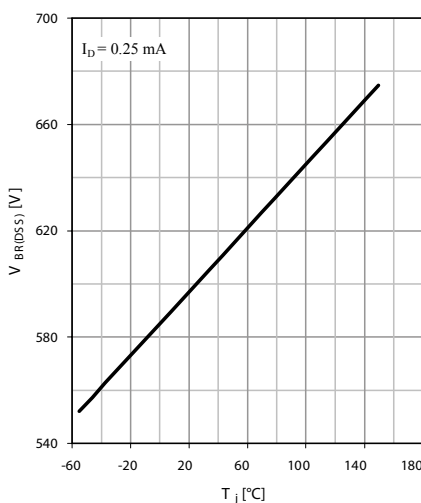


Fig. 11 Drain-source breakdown voltage

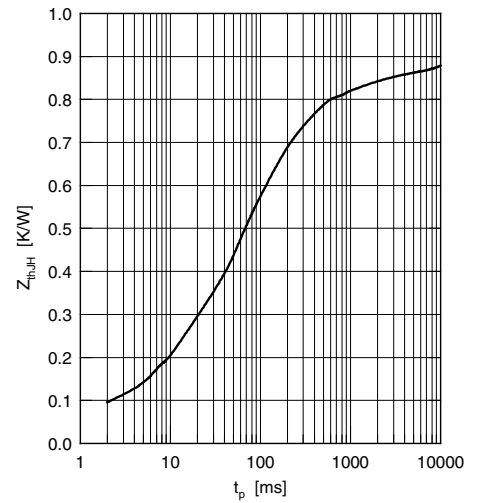


Fig. 12 Typ. transient thermal impedance with heat transfer paste



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