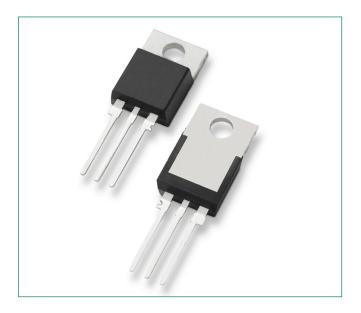


MCR72-3, MCR72-6, MCR72-8





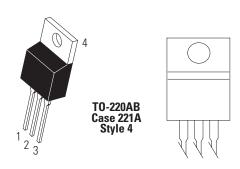
Description

Designed for industrial and consumer applications such as temperature, light and speed control; process and remote controls; warning systems; capacitive discharge circuits and MPU interface.

Features

- Center Gate Geometry for Uniform Current Density
- All Diffused and Glass-Passivated Junctions for Parameter Uniformity and Stability
- Small, Rugged
 Thermowatt Construction for Low Thermal
 Resistance, High Heat
 Dissipation and Durability
- Low Trigger Currents, 200
 µA Maximum for Direct
 Driving from Integrated
 Circuits
- These are Pb-Free Devices

Pin Out



Functional Diagram



Additional Information







Thyristors 8Amps Sen SCR

Maximum Ratings $(T_J = 25^{\circ}C \text{ unless otherwise noted})$

Rating		Symbol	Value	Unit
Peak Repetitive Off-State Voltage (Note 1) (- 40 to 110°C, Sine Wave, 50 to 60 Hz, Gate Open)	MCR72-3 MCR72-6 MCR72-8	V _{DRM} , V _{RRM}	100 400 600	V
On-State RMS Current (180° Conduction Angles; T _C = 83°C)		I _{T (RMS)}	8.0	А
Peak Non-Repetitive Surge Current (1/2 Cycle, Sine Wave 60 Hz, $T_J = 110$ °C		I _{TSM}	100	А
Circuit Fusing Consideration (t = 8.3 ms)		l²t	40	A²s
Forward Peak Gate Voltage (Pulse Width ≤ 10 µsec, T _C = 83°C)		V _{GM}	±5.0	V
Forward Peak Gate Current (Pulse Width ≤ 10 µsec, T _c = 83°C)		I _{GM}	1.0	А
Forward Peak Gate Power (Pulse Width ≤ 10 µsec, T _C = 83°C)		P _{GM}	5.0	W
Average Gate Power (t = 8.3 ms, $T_c = 83^{\circ}C$)		P _{G(AV)}	0.75	W
Operating Junction Temperature Range		T,	-40 to +110	°C
Storage Temperature Range		T _{stg}	-40 to +150	°C
Mounting Torque		-	8.0	in. lb.

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. V_{DBM} and V_{SBM} for all types can be applied on a continuous basis. Ratings apply for zero or negative gate voltage; however, positive gate voltage shall not be applied concurrent with negative potential on the anode. Blocking voltages shall not be tested with a constant current source such that the voltage ratings of the devices are exceeded.

Thermal Characteristics

Characterstic	Symbol	Value	Unit		
Thermal Resistance, Junction-to-Case	R _{euc}	2.2	°C / / /		
Thermal Resistance, Junction-to-Ambient	R _{eJA}	60	°C/W		
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T _L	260	°C		

Electrical Characteristics - **OFF** $(T_j = 25^{\circ}C \text{ unless otherwise noted})$

Characteristic		Symbol	Min	Тур	Max	Unit
Peak Repetitive Blocking Current	T _J = 25°C	I _{DRM}	-	-	10	
$(V_{AK} = V_{DRM} = V_{RRM}; R_{GK} = 1K\Omega)$	T _J = 110°C	IRRM	-	-	500	μΑ
High Logic Level Supply Current from V _{cc}		I _{CCH}	4	4	-	

Electrical Characteristics - **ON** $(T_J = 25^{\circ}C \text{ unless otherwise noted})$

Characteristic	Symbol	Min	Тур	Max	Unit
Peak Forward On–State Voltage ($I_{TM} = 16 \text{ A Peak}$, Pulse Width $\leq 1 \text{ ms}$, Duty Cycle $\leq 2\%$)	V _{TM}	-	1.7	2.0	V
Gate Trigger Current (Continuous dc) (Note 3) ($V_D = 12 \text{ V}; R_L = 100 \Omega$)	I _{GT}	_	30	200	μΑ
Gate Trigger Voltage (Continuous dc) (Note 3) ($V_D = 12 \text{ V}; R_L = 100 \Omega$)	V _{GT}	_	0.5	1.5	V
Gate Trigger Non-Trigger Voltage ($V_D = 12 \text{ Vdc}$, $R_L = 100 \Omega$, $T_J = 110^{\circ}\text{C}$)	V _{GD}	0.1	_	_	V
Holding Current ($V_D = 12 \text{ V, Initiating Current} = 200 \text{ mA, RGK} = 1 \text{k}\Omega$)	I _H	_	-	6.0	mA
Gate Controlled Turn-On Time (Note 5) $(V_D = Rated V_{DRM'} _{TM} = 16 \text{ A, } _{G} = 2 \text{ mA})$	t _{gt}	-	1.0	_	μs



Dynamic Characteristics

Characteristic	Symbol	Min	Тур	Max	Unit
Critical Rate-of-Rise of Off-State Voltage ($V_D = Rated V_{DBM}$, Exponential Waveform, Gate Open, $T_L = 110$ °C)	dv/dt	-	10	-	V/µs

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under

- 2. Ratings apply for negative gate voltage or R_{3x} = 1KΩ. Devices shall not have a positive gate voltage concurrently with a negative voltage on the anode. Devices should not be tested with a constant current source for forward and reverse blocking capability such that the voltage applied exceeds the rated blocking voltage.
- 3. RGK current not included in measurement.

Voltage Current Characteristic of SCR

Symbol	Parameter
V_{DRM}	Peak Repetitive Forward Off State Voltage
I _{DRM}	Peak Forward Blocking Current
V _{RRM}	Peak Repetitive Reverse Off State Voltage
I _{RRM}	Peak Reverse Blocking Current
V _{TM}	Maximum On State Voltage
I _H	Holding Current

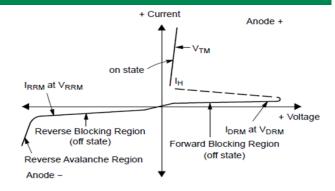
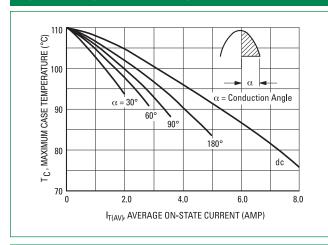


Figure 1. Average Current Derating





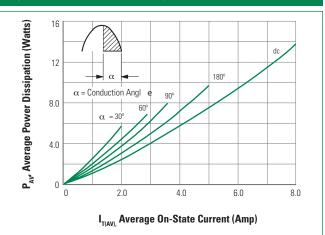


Figure 3. Normalized Gate Current

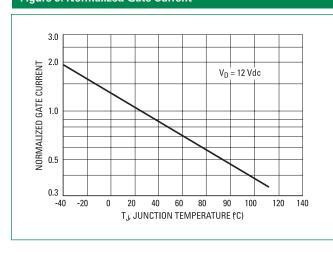
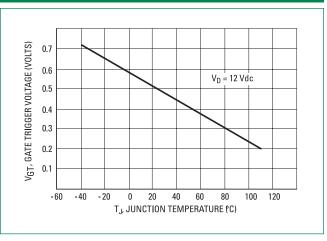


Figure 4. Gate Voltage



Part Marking System

MCR72-xG

=Device Code =Year

=Lot Trace Code

=Pb-Free Package

=Month

MCR72-x

Μ

G

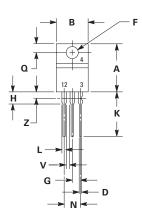
XXX

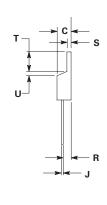


Dimensions

TO-220 Case 221A-01 Issue O

TO-220 Case 221A-09 Issue AH





Pin Assignment

Dim	Inc	hes	Millin	neters
Dim	Min	Max	Min	Max
Α	0.590	0.620	14.99	15.75
В	0.380	0.420	9.65	10.67
С	0.178	0.188	4.52	4.78
D	0.025	0.035	0.64	0.89
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.41	2.67
Н	0.110	0.130	2.79	3.30
J	0.018	0.024	0.46	0.61
K	0.540	0.575	13.72	14.61
L	0.060	0.075	1.52	1.91
N	0.195	0.205	4.95	5.21
Q	0.105	0.115	2.67	2.92
R	0.085	0.095	2.16	2.41
S	0.045	0.060	1.14	1.52
Т	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045		1.15	
Z		0.080		2.04

1	DIMENSIONING.	ANDTOL	FRANCING	PER ANGI	V14 5M	1022
١.	DIMENSIONING	AND IOL	ENAINCING	LEU HIAN	1 14.3101,	1302.

1	Cathode
2	Anode
3	Gate
4	Anode

XXX

G

MCR72-6TG YMXXX

MCR72-6T =Device Code

=Month

=Lot Trace Code

=Pb-Free Package

Ordering Information						
Device	Package	Shipping				
MCR72-3G						
MCR72-6G	TO 000AD					
MCR72-6TG	TO-220AB (Pb-Free)	1000 Units / Box				
MCR72-8G	(1 5-1166)					
MCR72-8TG						

^{2.} CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.