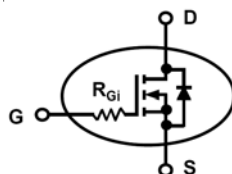


High Voltage Power MOSFET

IXTL2N450

(Electrically Isolated Tab)

N-Channel Enhancement Mode

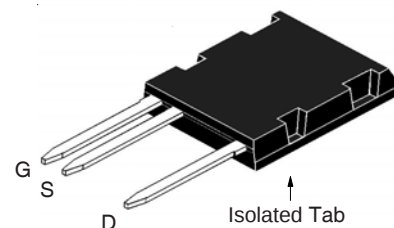


$$V_{DSS} = 4500V$$

$$I_{D25} = 2A$$

$$R_{DS(on)} \leq 20\Omega$$

ISOPLUS i5-Pak™



G = Gate
D = Drain

S = Source

Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ\text{C}$ to 150°C	4500	V
V_{DGR}	$T_J = 25^\circ\text{C}$ to 150°C , $R_{GS} = 1M\Omega$	4500	V
V_{GSS}	Continuous	± 20	V
V_{GSM}	Transient	± 30	V
I_{D25}	$T_C = 25^\circ\text{C}$	2	A
I_{DM}	$T_C = 25^\circ\text{C}$, Pulse Width Limited by T_{JM}	8	A
P_D	$T_C = 25^\circ\text{C}$	220	W
T_J		- 55 ... +150	$^\circ\text{C}$
T_{JM}		150	$^\circ\text{C}$
T_{stg}		- 55 ... +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ\text{C}$
T_{SOLD}	Plastic Body for 10s	260	$^\circ\text{C}$
F_C	Mounting Force	20..120 / 4.5..27	N/lb.
V_{ISOL}	50/60Hz, 1 Minute	4000	V~
Weight		8	g

Features

- Silicon Chip on Direct-Copper Bond (DCB) Substrate
- Isolated Mounting Surface
- 4000V~ RMS Electrical Isolation
- Molding Epoxies meet UL 94 V-0 Flammability Classification

Advantages

- Easy to Mount
- Space Savings
- High Power Density

Applications

- High Voltage Power Supplies
- Capacitor Discharge Applications
- Pulse Circuits
- Laser and X-Ray Generation Systems

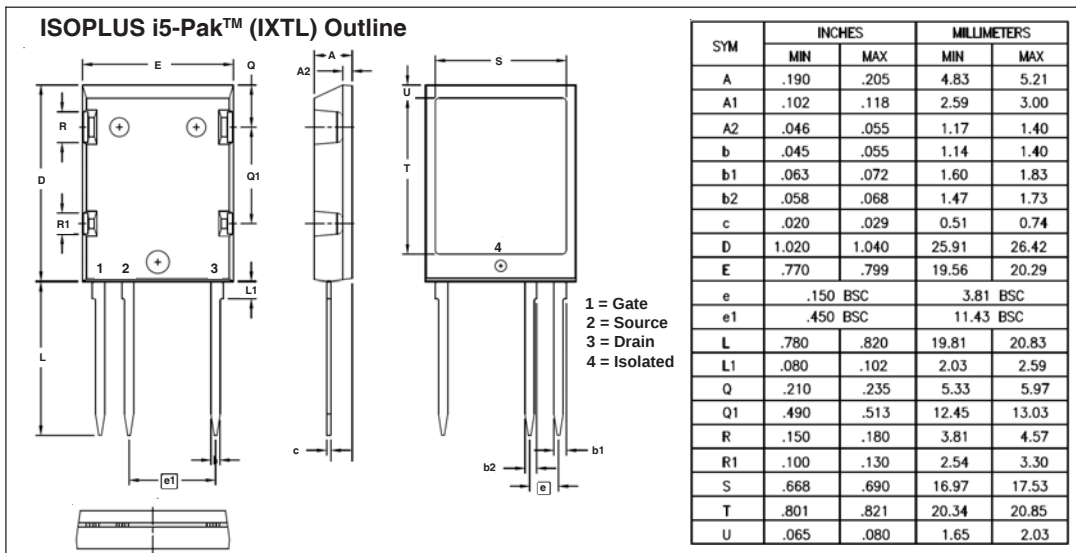
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu\text{A}$	3.5		6.0 V
I_{GSS}	$V_{GS} = \pm 20V$, $V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = 3.6kV$, $V_{GS} = 0V$			10 μA
	$V_{DS} = 4.5kV$			50 μA
	$V_{DS} = 3.6kV$ Note 2, $T_J = 125^\circ\text{C}$	250		μA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			20 Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 60\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	2.1	3.5	S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		6860	pF
C_{oss}			267	pF
C_{rss}			105	pF
R_{Gi}	Integrated Gate Input Resistance		4.0	Ω
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 1\text{kV}$, $I_D = 1\text{A}$ $R_G = 0\Omega$ (External)		40	ns
t_r			34	ns
$t_{d(off)}$			123	ns
t_f			205	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 1\text{kV}$, $I_D = 0.5 \cdot I_{D25}$		180	nC
Q_{gs}			34	nC
Q_{gd}			83	nC
R_{thJC}			0.56	$^\circ\text{C/W}$
R_{thCS}		0.15		$^\circ\text{C/W}$

Source-Drain Diode

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, Unless Otherwise Specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			2 A
I_{SM}	Repetitive, Pulse Width Limited by T_{JM}			8 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			3 V
t_{rr}	$I_F = 2\text{A}$, $-di/dt = 100\text{A}/\mu\text{s}$, $V_R = 100\text{V}$	1.75		μs

- Notes: 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.
 2. Part must be heatsunk for high-temp I_{dss} measurement.



IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338 B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

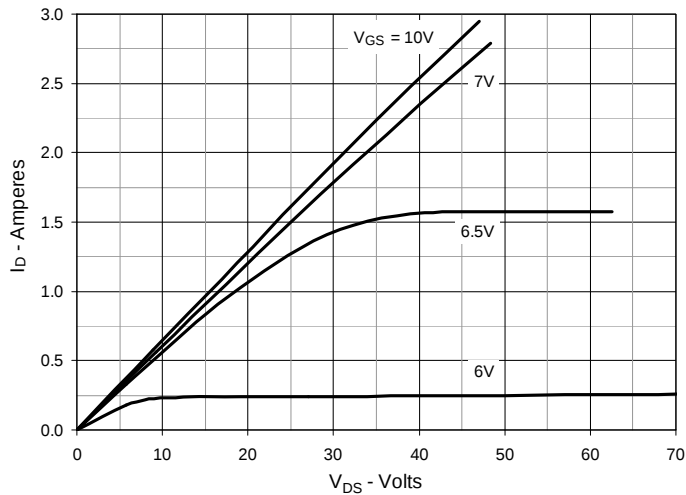
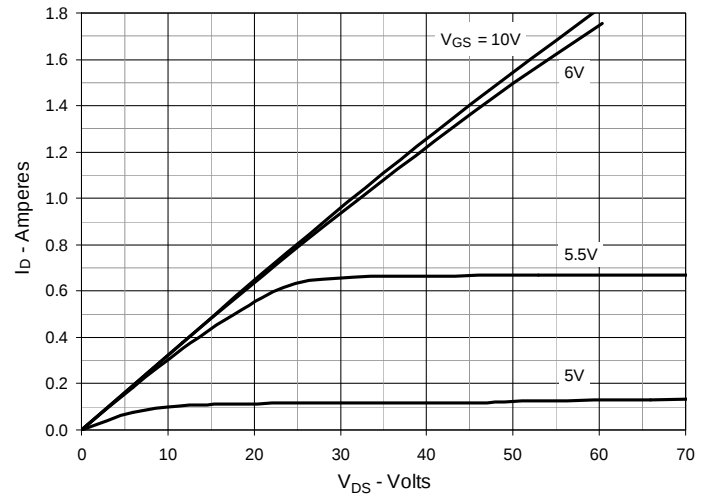
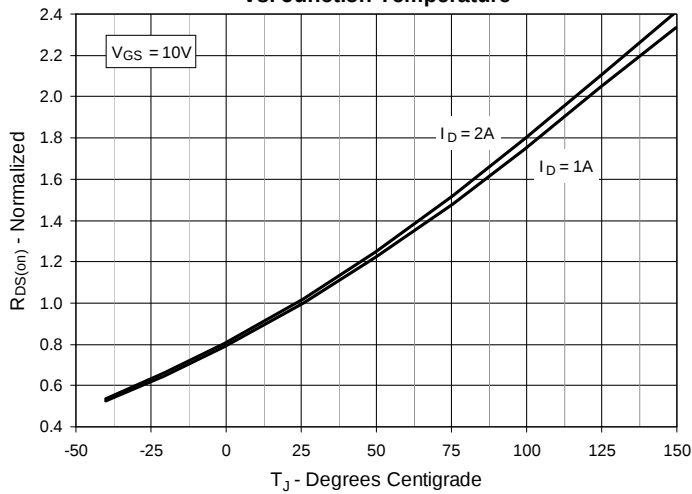
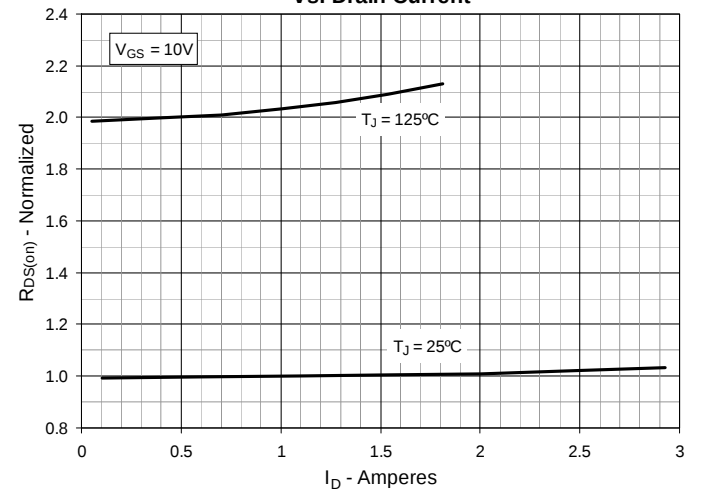
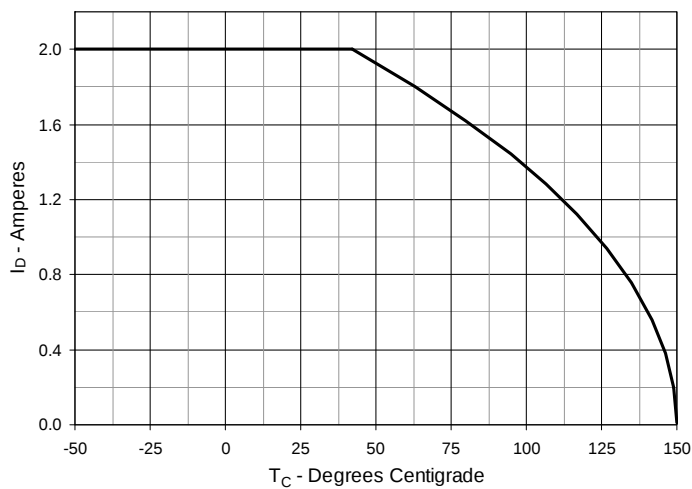
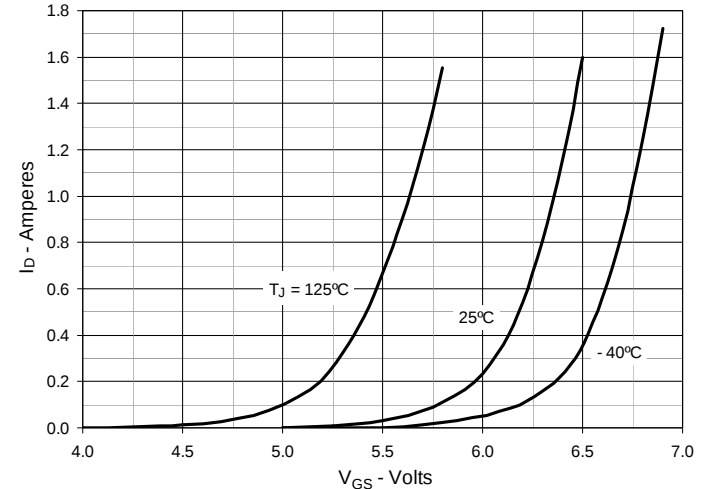
Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

Fig. 2. Output Characteristics @ $T_J = 125^\circ\text{C}$

Fig. 3. $R_{DS(on)}$ Normalized to $I_D = 1\text{A}$ Value vs. Junction Temperature

Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 1\text{A}$ Value vs. Drain Current

Fig. 5. Maximum Drain Current vs. Case Temperature

Fig. 6. Input Admittance


Fig. 7. Transconductance

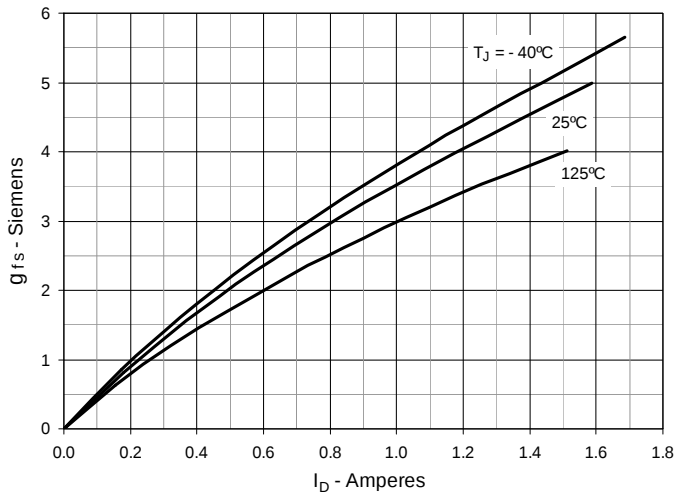


Fig. 8. Forward Voltage Drop of Intrinsic Diode

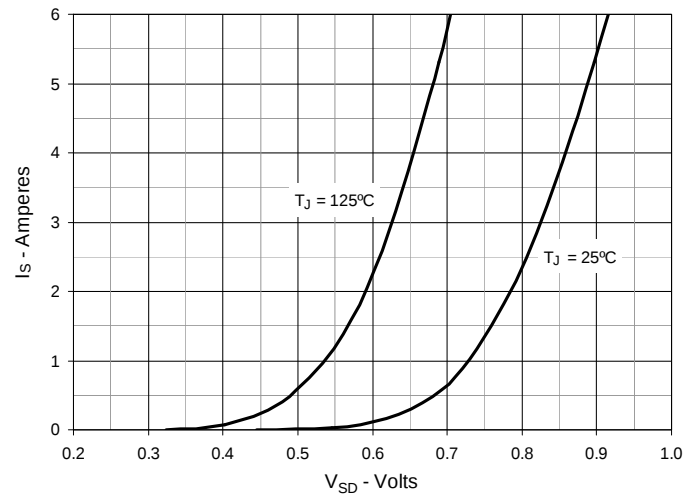


Fig. 9. Gate Charge

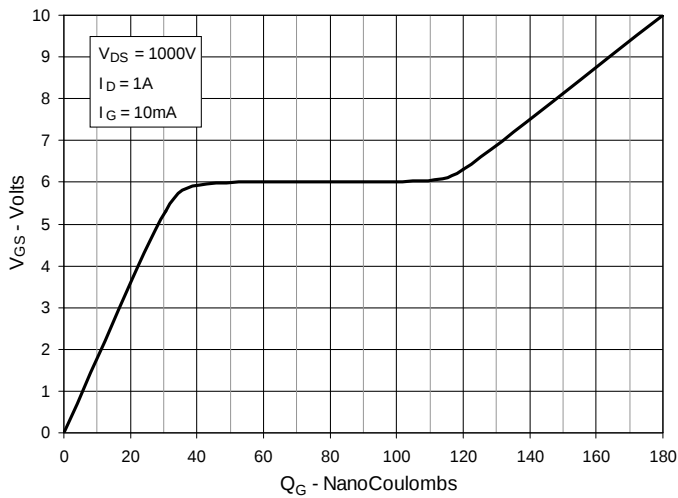


Fig. 10. Capacitance

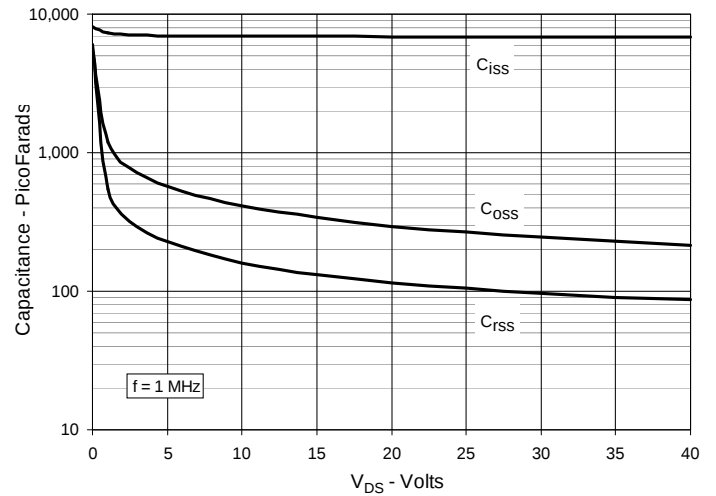


Fig. 11. Forward-Bias Safe Operating Area

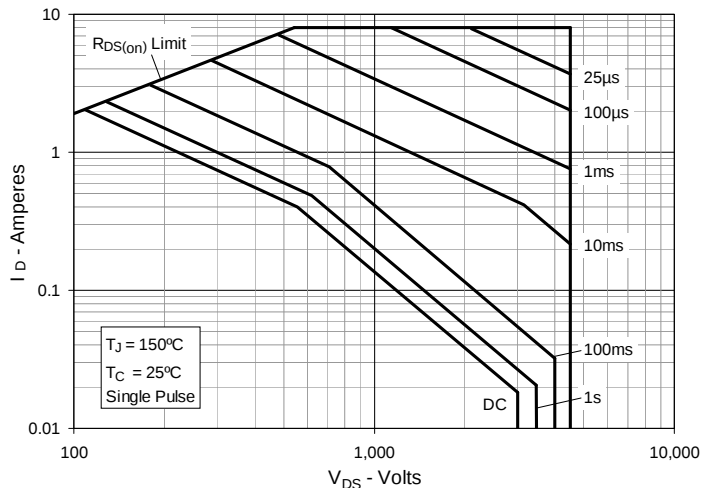


Fig. 12. Resistive Switching Times vs. External Gate Resistance

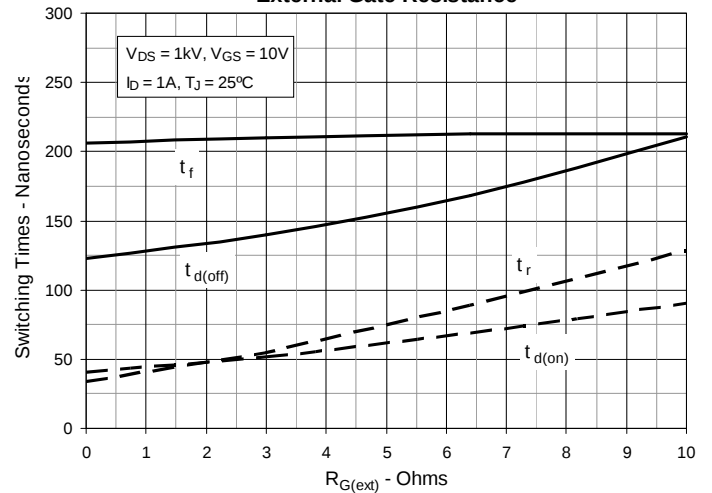
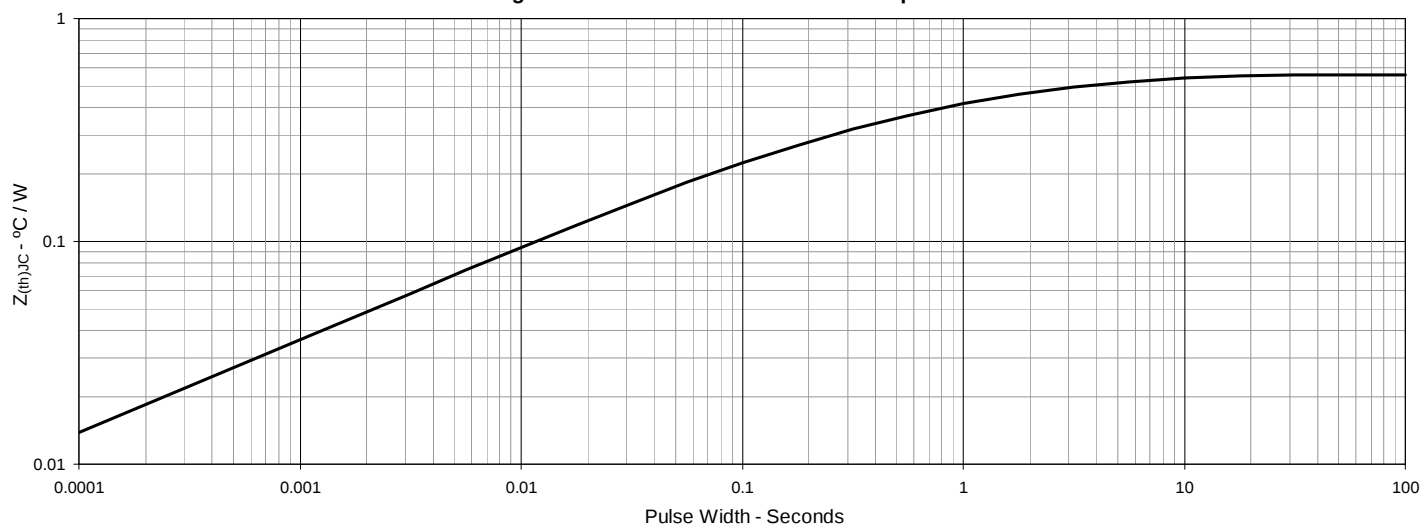


Fig. 13. Maximum Transient Thermal Impedance





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