

High Efficiency Thyristor

$$V_{RRM} = 1200\text{ V}$$

$$I_{TAV} = 50\text{ A}$$

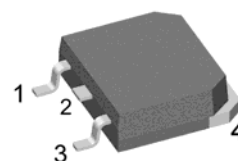
$$V_T = 1,27\text{ V}$$

Single Thyristor

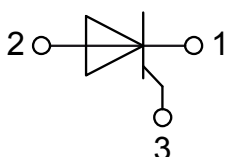
Part number

CLA50E1200TC

Marking on Product: CLA50E1200TC



Backside: anode



Features / Advantages:

- Thyristor for line frequency
- Planar passivated chip
- Long-term stability

Applications:

- Line rectifying 50/60 Hz
- Softstart AC motor control
- DC Motor control
- Power converter
- AC power control
- Lighting and temperature control

Package: TO-268AA (D3Pak)

- Industry standard outline
- RoHS compliant
- Epoxy meets UL 94V-0

Disclaimer Notice

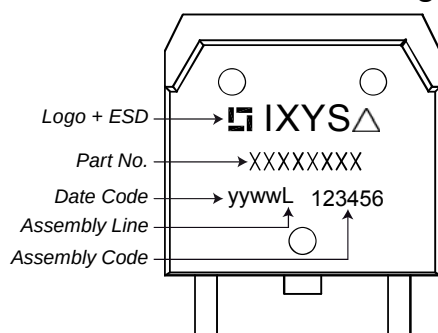
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Thyristor				Ratings			
Symbol	Definition	Conditions		min.	typ.	max.	Unit
$V_{RSM/DSM}$	max. non-repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$				1300	V
$V_{RRM/DRM}$	max. repetitive reverse/forward blocking voltage	$T_{VJ} = 25^{\circ}\text{C}$				1200	V
$I_{R/D}$	reverse current, drain current	$V_{R/D} = 1200\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			50	μA
		$V_{R/D} = 1200\text{ V}$	$T_{VJ} = 125^{\circ}\text{C}$			4	mA
V_T	forward voltage drop	$I_T = 50\text{ A}$	$T_{VJ} = 25^{\circ}\text{C}$			1,32	V
		$I_T = 100\text{ A}$				1,60	V
		$I_T = 50\text{ A}$	$T_{VJ} = 125^{\circ}\text{C}$			1,27	V
		$I_T = 100\text{ A}$				1,65	V
I_{TAV}	average forward current	$T_C = 125^{\circ}\text{C}$	$T_{VJ} = 150^{\circ}\text{C}$			50	A
$I_{T(RMS)}$	RMS forward current	180° sine				79	A
V_{T0}	threshold voltage	} for power loss calculation only	$T_{VJ} = 150^{\circ}\text{C}$			0,88	V
r_T	slope resistance					7,7	m Ω
R_{thJC}	thermal resistance junction to case					0,25	K/W
R_{thCH}	thermal resistance case to heatsink				0,15		K/W
P_{tot}	total power dissipation		$T_C = 25^{\circ}\text{C}$			500	W
I_{TSM}	max. forward surge current	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$			650	A
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			700	A
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}\text{C}$			555	A
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			595	A
I^2t	value for fusing	$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 45^{\circ}\text{C}$			2,12	kA ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			2,04	kA ² s
		$t = 10\text{ ms}; (50\text{ Hz}), \text{ sine}$	$T_{VJ} = 150^{\circ}\text{C}$			1,54	kA ² s
		$t = 8,3\text{ ms}; (60\text{ Hz}), \text{ sine}$	$V_R = 0\text{ V}$			1,48	kA ² s
C_j	junction capacitance	$V_R = 400\text{ V}$ $f = 1\text{ MHz}$	$T_{VJ} = 25^{\circ}\text{C}$		25		pF
P_{GM}	max. gate power dissipation	$t_p = 30\text{ }\mu\text{s}$	$T_C = 150^{\circ}\text{C}$			10	W
		$t_p = 300\text{ }\mu\text{s}$				5	W
P_{GAV}	average gate power dissipation					0,5	W
$(di/dt)_{cr}$	critical rate of rise of current	$T_{VJ} = 150^{\circ}\text{C}; f = 50\text{ Hz}$ repetitive, $I_T = 150\text{ A}$				150	A/ μs
		$t_p = 200\text{ }\mu\text{s}; di_G/dt = 0,3\text{ A}/\mu\text{s};$ $I_G = 0,3\text{ A}; V_D = \frac{2}{3} V_{DRM}$ non-repet., $I_T = 50\text{ A}$				500	A/ μs
$(dv/dt)_{cr}$	critical rate of rise of voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}\text{C}$			1000	V/ μs
		$R_{GK} = \infty$; method 1 (linear voltage rise)					
V_{GT}	gate trigger voltage	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			1,5	V
			$T_{VJ} = -40^{\circ}\text{C}$			1,6	V
I_{GT}	gate trigger current	$V_D = 6\text{ V}$	$T_{VJ} = 25^{\circ}\text{C}$			50	mA
			$T_{VJ} = -40^{\circ}\text{C}$			80	mA
V_{GD}	gate non-trigger voltage	$V_D = \frac{2}{3} V_{DRM}$	$T_{VJ} = 150^{\circ}\text{C}$			0,2	V
I_{GD}	gate non-trigger current					3	mA
I_L	latching current	$t_p = 10\text{ }\mu\text{s}$	$T_{VJ} = 25^{\circ}\text{C}$			125	mA
		$I_G = 0,3\text{ A}; di_G/dt = 0,3\text{ A}/\mu\text{s}$					
I_H	holding current	$V_D = 6\text{ V}$ $R_{GK} = \infty$	$T_{VJ} = 25^{\circ}\text{C}$			100	mA
t_{gd}	gate controlled delay time	$V_D = \frac{1}{2} V_{DRM}$	$T_{VJ} = 25^{\circ}\text{C}$			2	μs
		$I_G = 0,3\text{ A}; di_G/dt = 0,3\text{ A}/\mu\text{s}$					
t_q	turn-off time	$V_R = 100\text{ V}; I_T = 50\text{ A}; V_D = \frac{2}{3} V_{DRM}$ $T_{VJ} = 125^{\circ}\text{C}$ $di/dt = 10\text{ A}/\mu\text{s}$ $dv/dt = 20\text{ V}/\mu\text{s}$ $t_p = 200\text{ }\mu\text{s}$			200		μs

Package TO-268AA (D3Pak)			Ratings			
Symbol	Definition	Conditions	min.	typ.	max.	Unit
I_{RMS}	RMS current	per terminal			70	A
T_{VJ}	virtual junction temperature		-40		150	°C
T_{op}	operation temperature		-40		125	°C
T_{stg}	storage temperature		-40		150	°C
Weight				5		g
F_c	mounting force with clip		20		120	N

Product Marking



Part description

C = Thyristor (SCR)
 L = High Efficiency Thyristor
 A = (up to 1200V)
 50 = Current Rating [A]
 E = Single Thyristor
 1200 = Reverse Voltage [V]
 TC = TO-268AA (D3Pak) (2)

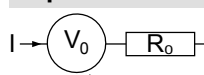
Ordering	Ordering Number	Marking on Product	Delivery Mode	Quantity	Code No.
Standard	CLA50E1200TC-TUB	CLA50E1200TC	Tube	30	502708
Alternative	CLA50E1200TC-TRL	CLA50E1200TC	Tape & Reel	400	502737

Similar Part	Package	Voltage class
CLA50E1200HB	TO-247AD (3)	1200

Equivalent Circuits for Simulation

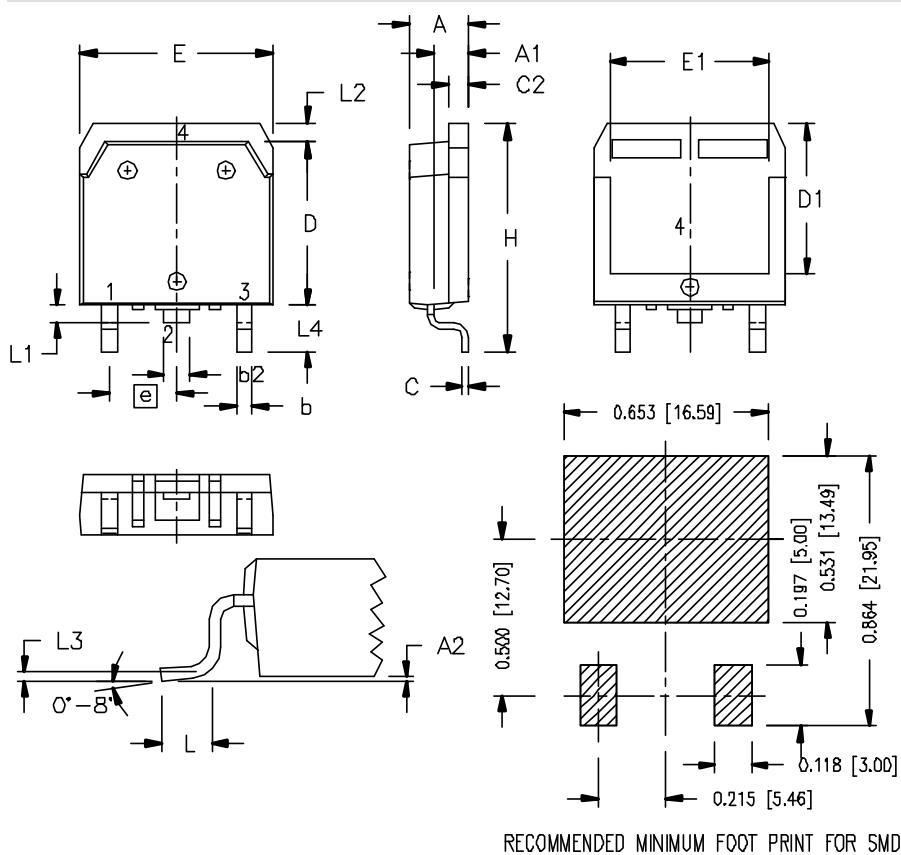
* on die level

$T_{VJ} = 150^{\circ}\text{C}$

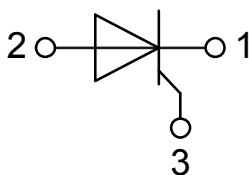


Thyristor

$V_{0\max}$	threshold voltage	0,88	V
$R_{0\max}$	slope resistance *	5,2	mΩ

Outlines TO-268AA (D3Pak)


Dim.	Millimeter		Inches	
	min	max	min	max
A	4.90	5.10	0.193	0.201
A1	2.70	2.90	0.106	0.114
A2	0.02	0.25	0.001	0.100
b	1.15	1.45	0.045	0.057
b2	1.90	2.10	0.075	0.083
C	0.40	0.65	0.016	0.026
C2	1.45	1.60	0.057	0.063
D	13.80	14.00	0.543	0.551
D1	12.40	12.70	0.488	0.500
E	15.85	16.05	0.624	0.632
E1	13.30	13.60	0.524	0.535
e	5.45 BSC		0.215 BSC	
H	18.70	19.10	0.736	0.752
L	2.40	2.70	0.094	0.106
L1	1.20	1.40	0.047	0.055
L2	1.00	1.15	0.039	0.045
L3	0.25 BSC		0.100 BSC	
L4	3.80	4.10	0.150	0.161



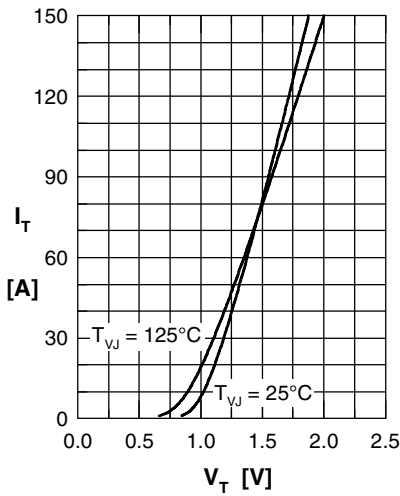
Thyristor


Fig. 1 Forward characteristics

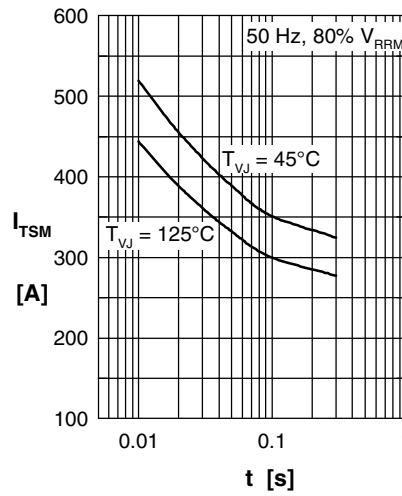
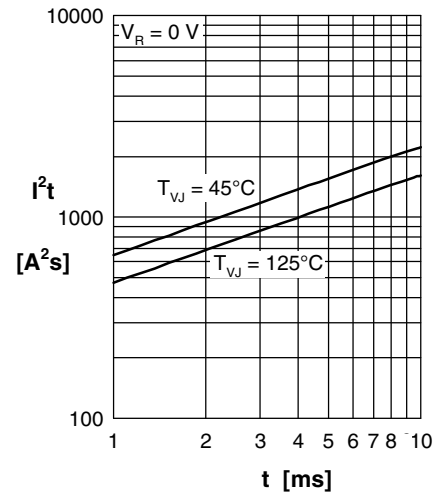
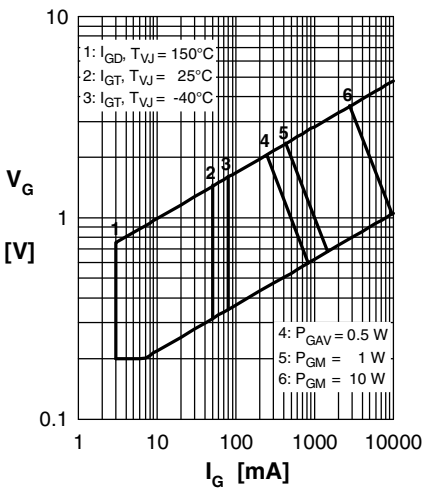

 Fig. 2 Surge overload current
 I_{TSM} : crest value, t : duration

 Fig. 3 I^2t versus time (1-10 s)


Fig. 4 Gate voltage & gate current

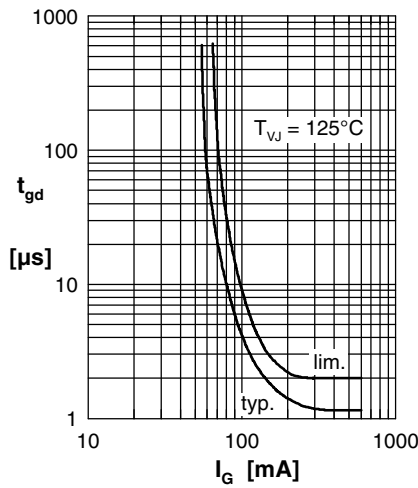
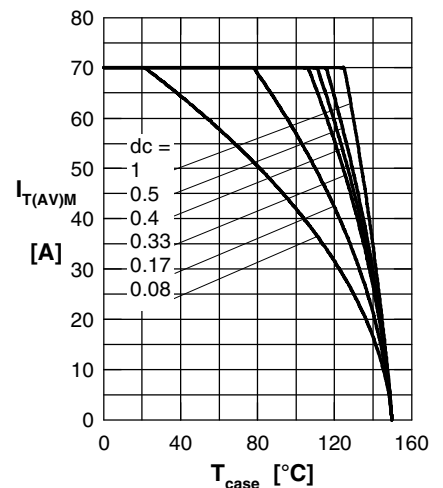

 Fig. 5 Gate controlled delay time t_{gd}


Fig. 6 Max. forward current at case temperature

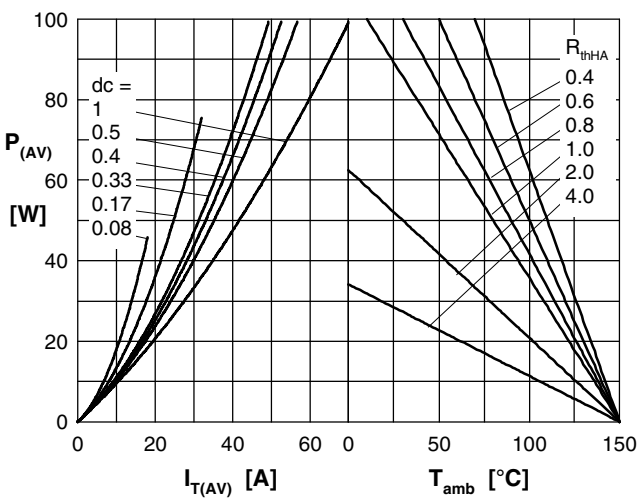
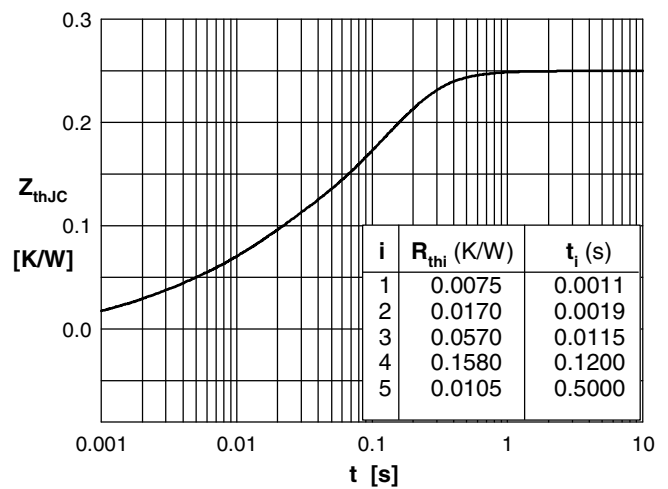

 Fig. 7a Power dissipation versus direct output current
 Fig. 7b and ambient temperature


Fig. 7 Transient thermal impedance junction to case