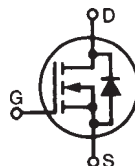


LinearL2™ Power MOSFET w/Extended FBSOA

IXTK60N50L2 IXTX60N50L2

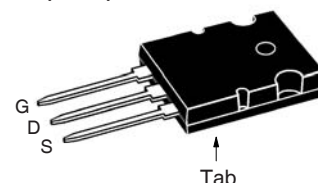
$V_{DSS} = 500V$
 $I_{D25} = 60A$
 $R_{DS(on)} \leq 100m\Omega$

N-Channel Enhancement Mode
Avalanche Rated

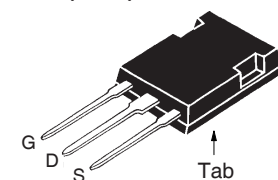


Symbol	Test Conditions	Maximum Ratings	
V_{DSS}	$T_J = 25^\circ C$ to $150^\circ C$	500	V
V_{DGR}	$T_J = 25^\circ C$ to $150^\circ C$, $R_{GS} = 1M\Omega$	500	V
V_{GSS}	Continuous	± 30	V
V_{GSM}	Transient	± 40	V
I_{D25}	$T_C = 25^\circ C$	60	A
I_{DM}	$T_C = 25^\circ C$, pulse width limited by T_{JM}	150	A
I_A	$T_C = 25^\circ C$	60	A
E_{AS}	$T_C = 25^\circ C$	3	J
P_D	$T_C = 25^\circ C$	960	W
T_J		-55...+150	$^\circ C$
T_{JM}		150	$^\circ C$
T_{stg}		-55...+150	$^\circ C$
T_L	Maximum Lead Temperature for Soldering	300	$^\circ C$
T_{SOLD}	1.6 mm (0.062in.) from Case for 10s	260	$^\circ C$
M_d	Mounting torque (IXTK)	1.13/10	Nm/lb.in
F_C	Mounting Force (IXTX)	20..120 / 4.5..27	N/lb
Weight	TO-264	10	g
	PLUS247	6	g

TO-264 (IXTK)



PLUS247 (IXTX)



G = Gate D = Drain
S = Source Tab = Drain

Features

- Designed for linear operation
- International standard packages
- Avalanche rated
- Guaranteed FBSOA at $75^\circ C$

Advantages

- Easy to mount
- Space savings
- High power density

Applications

- Solid state circuit breakers
- Soft start controls
- Linear amplifiers
- Programmable loads
- Current regulators

Symbol	Test Conditions ($T_J = 25^\circ C$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
BV_{DSS}	$V_{GS} = 0V$, $I_D = 1mA$	500		V
$V_{GS(th)}$	$V_{DS} = V_{GS}$, $I_D = 250\mu A$	2.5		4.5 V
I_{GSS}	$V_{GS} = \pm 30V$, $V_{DS} = 0V$			± 200 nA
I_{DSS}	$V_{DS} = V_{DSS}$, $V_{GS} = 0V$ $T_J = 125^\circ C$			50 μA 5 mA
$R_{DS(on)}$	$V_{GS} = 10V$, $I_D = 0.5 \cdot I_{D25}$, Note 1			100 m Ω

Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
g_{fs}	$V_{DS} = 10\text{V}$, $I_D = 0.5 \cdot I_{D25}$, Note 1	18	25	32 S
C_{iss}	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$		24	nF
C_{oss}			1325	pF
C_{rss}			172	pF
$t_{d(on)}$	Resistive Switching Times $V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$ $R_G = 0.5\Omega$ (External)		40	ns
t_r			40	ns
$t_{d(off)}$			165	ns
t_f			38	ns
$Q_{g(on)}$	$V_{GS} = 10\text{V}$, $V_{DS} = 0.5 \cdot V_{DSS}$, $I_D = 0.5 \cdot I_{D25}$		610	nC
Q_{gs}			130	nC
Q_{gd}			365	nC
R_{thJC}			0.13	$^\circ\text{C/W}$
R_{thCS}			0.15	$^\circ\text{C/W}$

Safe Operating Area Specification

Symbol	Test Conditions	Characteristic Values		
		Min.	Typ.	Max.
SOA	$V_{DS} = 400\text{V}$, $I_D = 1.1\text{A}$, $T_C = 75^\circ\text{C}$, $t_p = 3\text{s}$	440		W

Source-Drain Diode

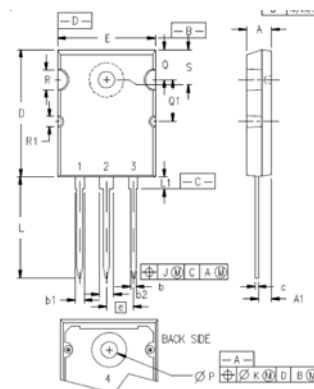
Symbol	Test Conditions ($T_J = 25^\circ\text{C}$, unless otherwise specified)	Characteristic Values		
		Min.	Typ.	Max.
I_S	$V_{GS} = 0\text{V}$			60 A
I_{SM}	Repetitive, pulse width limited by T_{JM}			240 A
V_{SD}	$I_F = I_S$, $V_{GS} = 0\text{V}$, Note 1			1.5 V
t_{rr}	$I_F = 60\text{A}$, $-di/dt = 100\text{A}/\mu\text{s}$, $V_R = 100\text{V}$, $V_{GS} = 0\text{V}$		980	ns
I_{RM}			73	A
Q_{RM}			35.8	μC

Notes: 1. Pulse test, $t \leq 300\mu\text{s}$, duty cycle, $d \leq 2\%$.

IXYS Reserves the Right to Change Limits, Test Conditions, and Dimensions.

IXYS MOSFETs and IGBTs are covered by one or more of the following U.S. patents:	4,835,592	4,931,844	5,049,961	5,237,481	6,162,665	6,404,065 B1	6,683,344	6,727,585	7,005,734 B2	7,157,338B2
	4,860,072	5,017,508	5,063,307	5,381,025	6,259,123 B1	6,534,343	6,710,405 B2	6,759,692	7,063,975 B2	
	4,881,106	5,034,796	5,187,117	5,486,715	6,306,728 B1	6,583,505	6,710,463	6,771,478 B2	7,071,537	

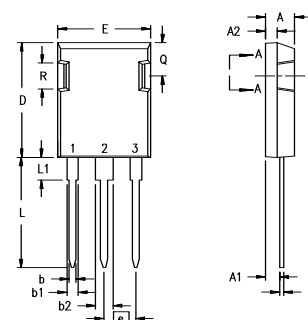
TO-264 (IXTK) Outline



Terminals: 1 - Gate
2,4 - Drain
3 - Source

SYM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.185	.209	4.70	5.31
A1	.102	.118	2.59	3.00
b	.037	.055	0.94	1.40
b1	.087	.102	2.21	2.59
b2	.110	.126	2.79	3.20
c	.017	.029	0.43	0.74
D	1.007	1.047	25.58	26.59
E	.760	.799	19.30	20.29
e	.215 BSC		5.46 BSC	
J	.006	.010	0.00	0.25
K	.006	.010	0.00	0.25
L	.779	.842	19.79	21.39
L1	.087	.102	2.21	2.59
Q	.122	.138	3.10	3.51
Q1	.240	.256	6.10	6.50
Q1	.330	.346	8.38	8.79
ØP	.155	.187	3.94	4.75
ØR1	.085	.093	2.16	2.36
S	.243	.253	6.17	6.43

PLUS 247™ (IXTX) Outline



Terminals: 1 - Gate
2 - Drain
3 - Source

Dim.	Millimeter		Inches	
	Min.	Max.	Min.	Max.
A	4.83	5.21	.190	.205
A ₁	2.29	2.54	.090	.100
A ₂	1.91	2.16	.075	.085
b	1.14	1.40	.045	.055
b ₁	1.91	2.13	.075	.084
b ₂	2.92	3.12	.115	.123
C	0.61	0.80	.024	.031
D	20.80	21.34	.819	.840
E	15.75	16.13	.620	.635
e	5.45 BSC		.215 BSC	
L	19.81	20.32	.780	.800
L1	3.81	4.32	.150	.170
Q	5.59	6.20	.220	0.244
R	4.32	4.83	.170	.190

Fig. 1. Output Characteristics @ $T_J = 25^\circ\text{C}$

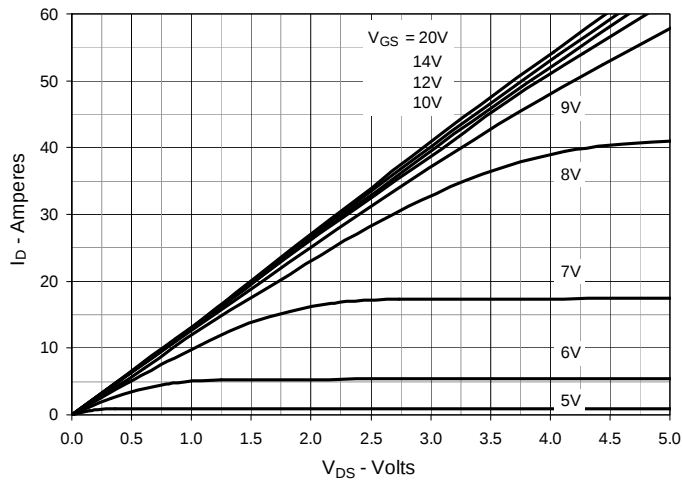


Fig. 2. Extended Output Characteristics @ $T_J = 25^\circ\text{C}$

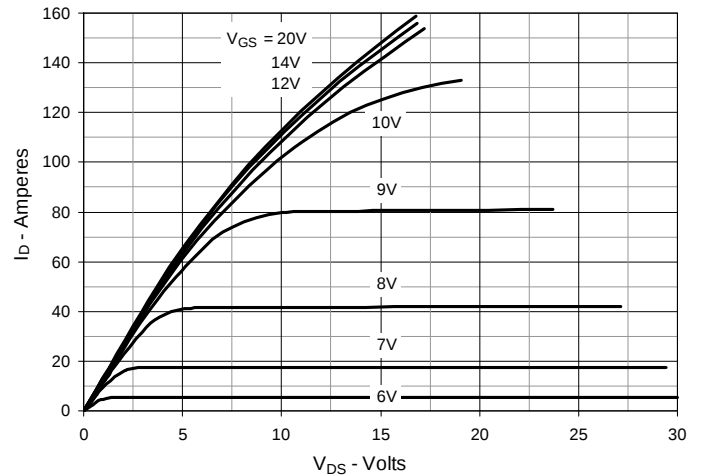


Fig. 3. Output Characteristics @ $T_J = 125^\circ\text{C}$

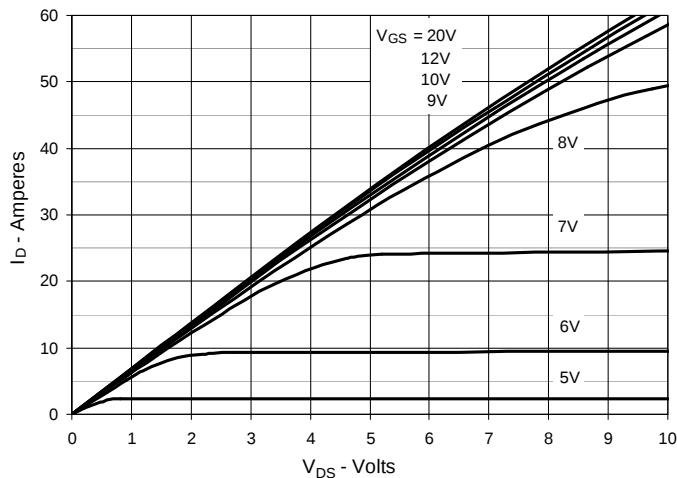


Fig. 4. $R_{DS(on)}$ Normalized to $I_D = 30\text{A}$ Value vs. Junction Temperature

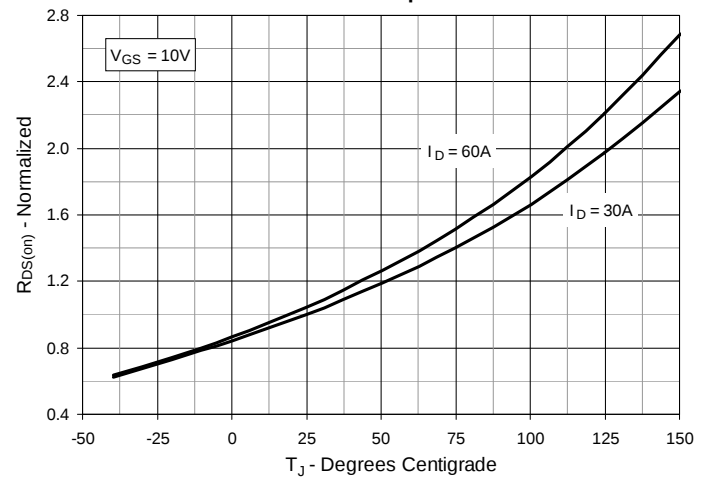


Fig. 5. $R_{DS(on)}$ Normalized to $I_D = 30\text{A}$ Value vs. Drain Current

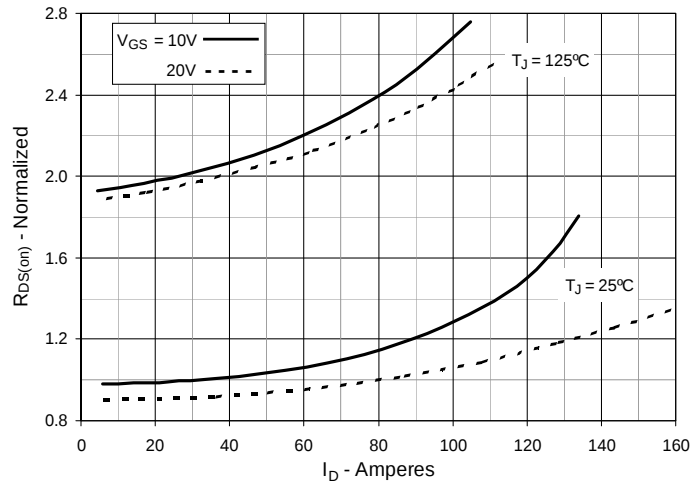


Fig. 6. Maximum Drain Current vs. Case Temperature

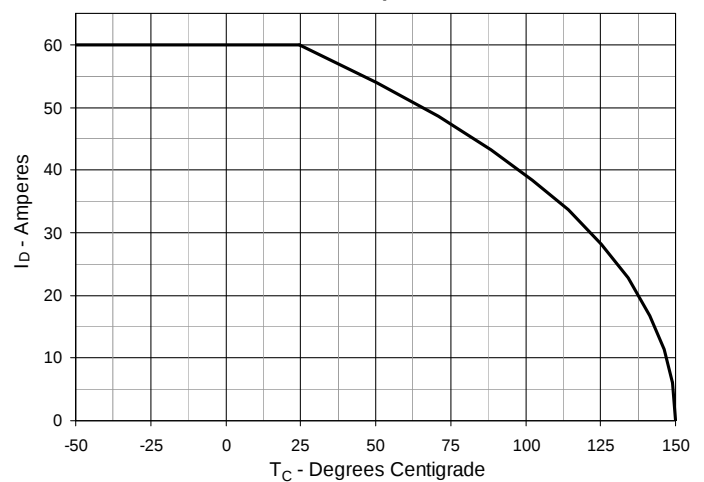


Fig. 7. Input Admittance

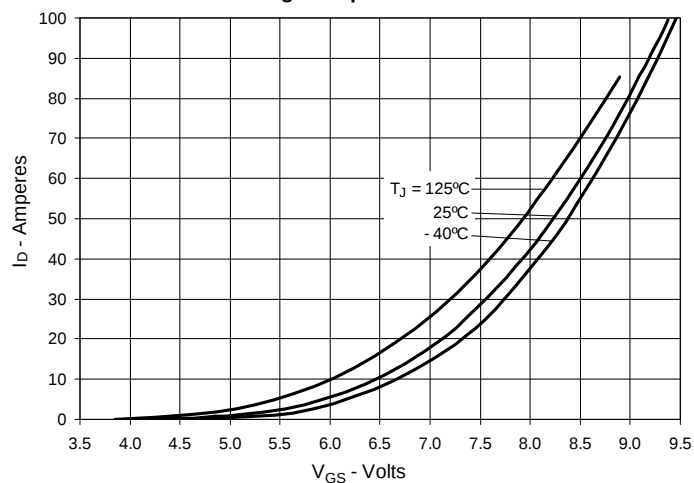


Fig. 8. Transconductance

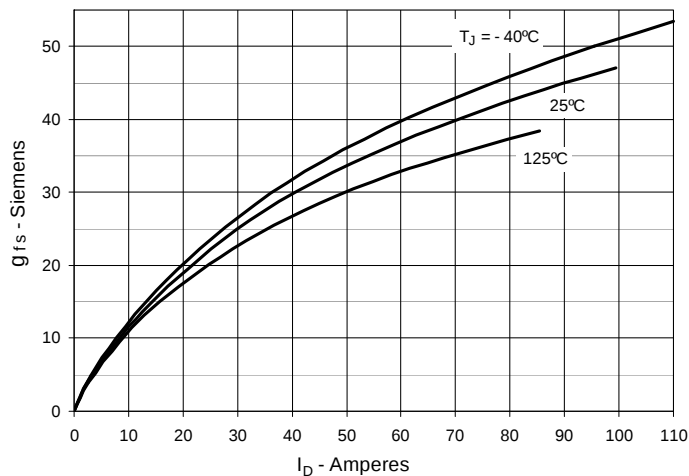


Fig. 9. Forward Voltage Drop of Intrinsic Diode

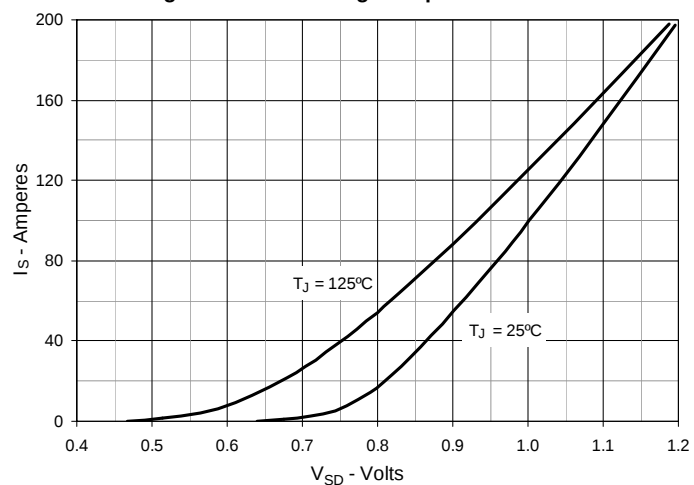


Fig. 10. Gate Charge

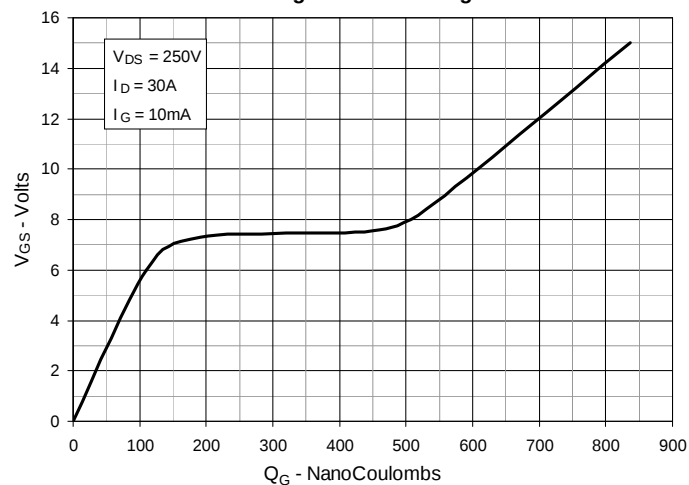


Fig. 11. Capacitance

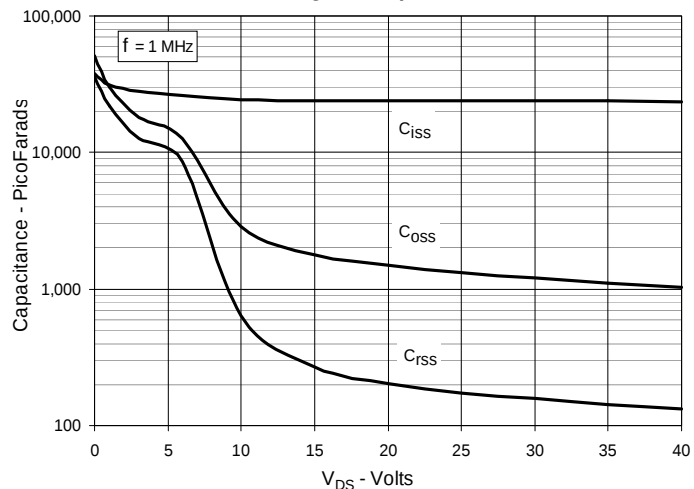


Fig. 12. Maximum Transient Thermal Impedance

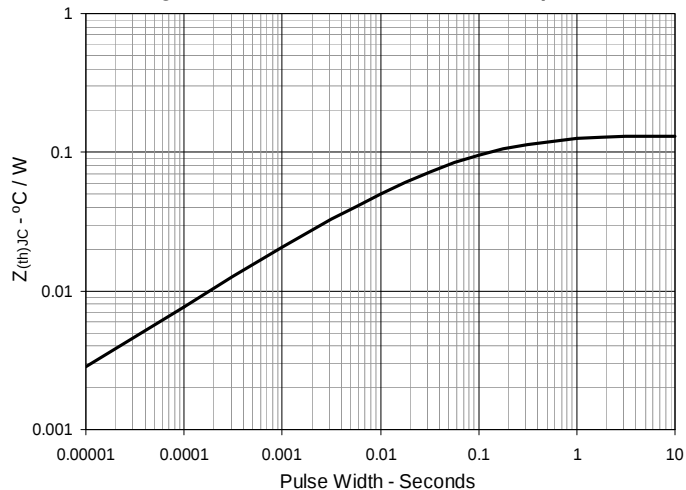


Fig. 13. Forward-Bias Safe Operating Area

@ $T_C = 25^\circ\text{C}$

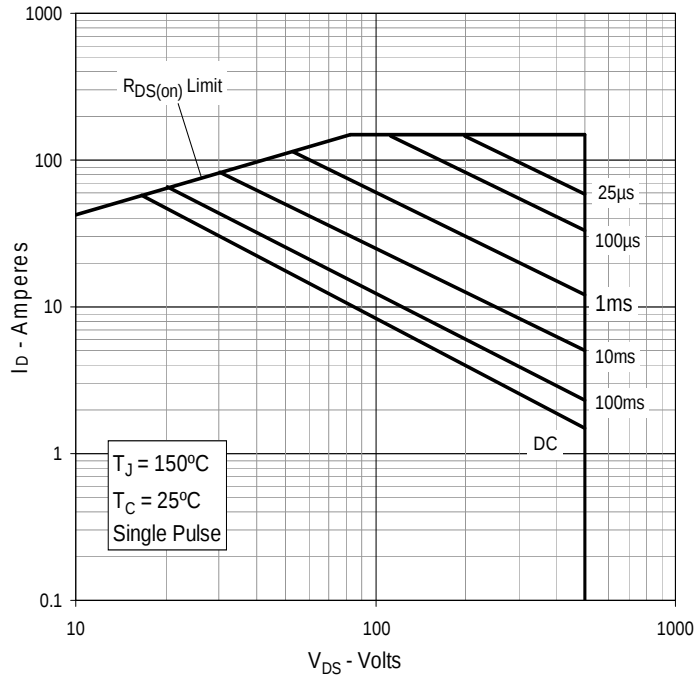
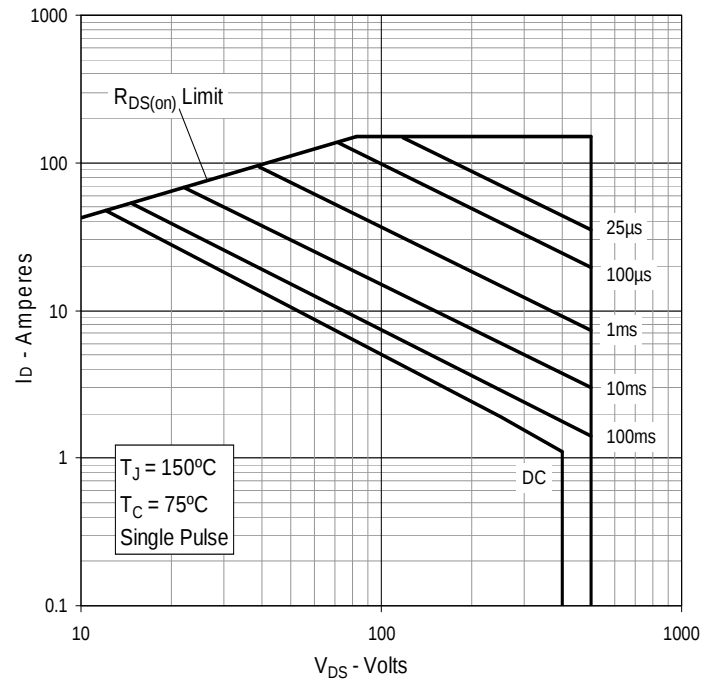


Fig. 14. Forward-Bias Safe Operating Area

@ $T_C = 75^\circ\text{C}$





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